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# Scope

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The purpose of this data book is to provide architectural, hardware and installation information for the **PROCStar III™** system.

This data book is organized in the following chapters:

1. **Introduction** – Product description and purpose.
2. **Key Features** – Main features and performance of the product.
3. **Standard Models** – Standard product models available.
4. **Architecture** – Product architecture, components, busses and clocks.
5. **DMA Controller** – DMA operation and performance.
6. **Connectors** – Product connectors' description and pinout.
7. **Memories** – Product memory structure.
8. **LEDs** – Product LEDs functions.
9. **Technical Specifications** - Electrical, mechanical and other technical specifications.
10. **Installation** – Product requirements and installation instructions.
11. **GiDEL Accessories** – GiDEL management software and IPs.
12. **Appendix** – Additional information.
13. **References**-List of referenced documents.
14. **Glossary** – Term definitions and acronyms
15. **Revision History** – Product and document revision history.



# 1. Introduction

---

The **PROCStar III**<sup>™</sup> system provides a high-capacity, high-speed FPGA-based platform along with high throughput and massive memory. This system is targeted at powerful system development, machine vision, imaging and high performance embedded computing applications.

The **PROCStar III** architecture, based on Altera's Stratix III FPGA technology, is capable of running at system speeds of up to 300 MHz.

The **PROCStar III** is 8-lane PCI Express hosted. The performance, memory and add-on daughterboards flexible architecture enable the system to meet large application needs. Eight SODIMM sockets provide up to 32 GB of DDR2 memory, in addition to 1GB on-board memory. The extensive memory conjoined with the fast PCIe connection enable strong co-processing between a PC with standard OS and the FPGA accelerator. Support an optional embedded CPU which offers an on-board immediate complex control.

The **PROCStar III** system, enhanced with GiDEL's **PROCDeveloper's Kit**<sup>™</sup> management software, offers an incredible improvement in time-to-market.

The PROCStar III system is suitable for the following applications:

- Vision, imaging and image recognition
- DSP
- System hardware acceleration
- Algorithm design and verification
- Aerospace and military systems
- Test equipment
- SoC prototyping and debugging

The ***PROCStar III*** system, the on-board controllers and the automatic code generation eliminate the need to:

- Design a high speed custom board with maximum flexibility
- Write a PCI Express driver
- Write an application driver layer
- Define board constraints
- Design memory controller
- Write environment FPGA code

This enables designers to focus on their proprietary value-added design instead of spending their valuable time recreating standard design components. The generated HDL code enables high speed, easy-to-use parallel access to large memories. User designs may be in HDL, C-based, Simulink (graphical design) or any combination of them.



## 2. Key Features

---

- Support up to 4 ALTERA Stratix III 80E, 110E, 150L or 260E or 340L FPGAs.
- 8-lane PCI Express host interface.
- Five-level memory structure \*:
  - ✓ Up to 27000 MLAB (320-bit) RAM blocks, embedded in FPGA\*
  - ✓ Up to 4160 M9K (9K-bit) RAM blocks, embedded in FPGA \*
  - ✓ Up to 192 M144K (144K-bit) RAM blocks, embedded in FPGA \*
  - ✓ Up to 4 large 256MB DDR2 on board memories \*
  - ✓ 8 DDR2 SODIMM modules with up to 4 GB each \*
- Typical system frequency of 100 - 325 MHz.
- Up to 32 DMA channels
- Up to 3584 of 18x18 bit multipliers implemented in Stratix III devices\*.
- Up to 5 PSDBs (PROCStar III Daughterboards) connections: Camera Link, machine I/Os, LVDS interface and other interfaces.
- Immediate and simple high bandwidth use of the on-board memories with the innovative GIDEL PROCMultiPort™ configurable IP (a part of GIDEL PROC Developer's Kit). Each memory can be used for parallel data streaming, and for debug data capture.
- Up to 12 TMS320C64 DSPs on future versions(on PSDBs)
- Flexible clocking System with two global clocks distributed, buffered and optimized for low skew.
- Volatile and non volatile design security
- Possibility for fast direct board to board connection via SODIMM sockets.
- Temperature monitoring and over temperature protection.
- Supported by GiDEL's PROC Developer's Kit management software.
- Drivers for Windows and Linux Operating Systems.

\*All values depend on the board model (Refer to Ch. 3: Standard Models ) and operating frequency (Refer to paragraph 2.1-PROCStar III Performance).

## 2.1. PROCStar III Performance

The *PROCStar III* system provides a high-performance FPGA-based platform with high throughput and massive memory. Table 1 and Table 2 describe the *PROCStar III* performance capabilities.

Table 1: PROCStarIII Memory Throughput

| Memory Structure | Capacity         | Typical Performance* | Throughput* |
|------------------|------------------|----------------------|-------------|
| Embedded in FPGA | 4160xM9K Blocks  | 300 MHz              | 11,000 GB/s |
| Embedded in FPGA | 192xM144K Blocks | 300 MHz              | 1,000 GB/s  |
| On-Board Memory  | 4x256MB DDR2     | 667 MHz (DDR)        | 16 GB/s     |
| SODIMM Modules   | 8x4G DDR2        | 360 MHz(DDR)         | 17 GB/s     |

\* Refer to the Appendix for throughput calculations (paragraph 12.1)

Table 2: Processing Performance Examples

| Algorithm   | Data Flow Rate                   | % of one FPGA Logic Critical Resource* |       |       |
|---|----------------------------------|--|-------|-------|
|   |                                  | 80E                                    | 110E  | 150L  |
| <b>1024*1024 FFT</b><br>(12 bit width)  | 370MHz<br>(Transform time 5.7ms) | 11%                                    | 8.2%  | 10%   |
| <b>9*9 symmetric filter</b><br>(12 bit data,<br>16 bit coefficients)            | 336MB/s                          | 1%                                     | <1%   | <1%   |
| <b>7*7 8 bit Median filter</b>  | 255MHz                           | 11%                                    | 8.4%  | 6.3%  |
| <b>Open/Close circle</b><br>with radius up to 15<br>pixels<br>(8 bit per pixel) | 323MHz                           | 5%                                     | 3.8%  | 2.9%  |
| Threshold, add,<br>subtract, 10 → 8 LUT   | >> 300MHz                        | << 1%                                  | << 1% | << 1% |

\* Efficient utilization is expected with a full resource design.



### 3. Standard Models

This chapter details the standard **PROCStar III** models available.

The model names have the following structure: **PROCStar III XX-YZP** where:

**XX:** Type of Stratix III devices: 80E, 110E, 150L, 260E or 340L.

**Y:** Number of Stratix III devices installed: 1, 2 or 4.

**Z:** Speed grade: **A** = -2 speed grade..

**B** = -3 speed grade

**P:** Power model: **Blank** = Standard Model.

**P** = high power models. Available for 260E and 340L devices.

The high power models are used when high logic performance and utilization is required. Note that the P model board is constructed with heat sinks and thus occupies two PCIe computer slots.

For information on P-modules power consumption and working conditions, see **Figure 14: PROCStar III Operating Conditions**.

The following table lists the available PROCStar III models:

**Table 3: GiDEL PROCStar III Standard Models**

| Ordering Code<br>(Basic Models) | Stratix III<br>Device | Speed<br>Grade | # of<br>FPGAs | On-Board<br>DDR II | DDR II<br>SODIMM<br>Sockets | FPGA Internal<br>RAM<br>(Kbits) | LEs*   |
|---------------------------------|-----------------------|----------------|---------------|--------------------|-----------------------------|---------------------------------|--------|
| <b>PROCStarIII</b> 80E-1B       | EP3SE80               | -3             | 1             | 256MB              | 2                           | 7183                            | 80K    |
| <b>PROCStarIII</b> 80E-2B       | EP3SE80               | -3             | 2             | 512MB              | 4                           | 14366                           | 160K   |
| <b>PROCStarIII</b> 80E-4B       | EP3SE80               | -3             | 4             | 1024MB             | 8                           | 28732                           | 320K   |
| <b>PROCStarIII</b> 110E-1A      | EP3SE110              | -2             | 1             | 256MB              | 2                           | 9399                            | 107.5K |
| <b>PROCStarIII</b> 110E-2A      | EP3SE110              | -2             | 2             | 512MB              | 4                           | 18798                           | 215K   |
| <b>PROCStarIII</b> 110E-4A      | EP3SE110              | -2             | 4             | 1024MB             | 8                           | 37596                           | 430K   |
| <b>PROCStarIII</b> 110E-1B      | EP3SE110              | -3             | 1             | 256MB              | 2                           | 9399                            | 107.5K |
| <b>PROCStarIII</b> 110E-2B      | EP3SE110              | -3             | 2             | 512MB              | 4                           | 18798                           | 215K   |
| <b>PROCStarIII</b> 110E-3B      | EP3SE110              | -3             | 3             | 768MB              | 6                           | 28197                           | 322.5  |
| <b>PROCStarIII</b> 110E-4B      | EP3SE110              | -3             | 4             | 1024MB             | 8                           | 37596                           | 430K   |
| <b>PROCStarIII</b> 150L-1B      | EP3SL150              | -3             | 1             | 256MB              | 2                           | 7280                            | 142.5K |
| <b>PROCStarIII</b> 150L-2B      | EP3SL150              | -3             | 2             | 512MB              | 4                           | 14560                           | 285K   |
| <b>PROCStarIII</b> 150L-4B      | EP3SL150              | -3             | 4             | 1024MB             | 8                           | 29120                           | 570K   |
| <b>PROCStarIII</b> 260E-1A      | EP3SE260              | -2             | 1             | 256MB              | 2                           | 17876                           | 255K   |
| <b>PROCStarIII</b> 260E-2A      | EP3SE260              | -2             | 2             | 512MB              | 4                           | 35752                           | 510K   |

(Table continued on next page)

Table 4: GiDEL PROCStar III Standard Models(Continued)

| Ordering Code<br>(Basic Models) | Stratix III<br>Device | Speed<br>Grade | # of<br>FPGAs | On-Board<br>DDR II | DDR II<br>SODIMM<br>Sockets | FPGA Internal<br>RAM<br>(Kbits) | LEs*   |
|---------------------------------|-----------------------|----------------|---------------|--------------------|-----------------------------|---------------------------------|--------|
| <i>PROCStarIII</i> 260E-4A      | EP3SE260              | -2             | 4             | 1024MB             | 8                           | 71504                           | 1020K  |
| <i>PROCStarIII</i> 260E-1B      | EP3SE260              | -3             | 1             | 256MB              | 2                           | 17876                           | 255K   |
| <i>PROCStarIII</i> 260E-2B      | EP3SE260              | -3             | 2             | 512MB              | 4                           | 35752                           | 510K   |
| <i>PROCStarIII</i> 260E-4B      | EP3SE260              | -3             | 4             | 1024MB             | 8                           | 71504                           | 1020K  |
| <i>PROCStarIII</i> 340L-1B      | EPS3SL340             | -3             | 1             | 256MB              | 2                           | 20491                           | 337.5K |
| <i>PROCStarIII</i> 340L-2B      | EPS3SL340             | -3             | 2             | 512MB              | 4                           | 40982                           | 675K   |
| <i>PROCStarIII</i> 340L-4B      | EPS3SL340             | -3             | 4             | 1024MB             | 8                           | 81964                           | 1350K  |
| <i>PROCStarIII</i> 260E-1AP     | EP3SE260              | -2             | 1             | 256MB              | 2                           | 17876                           | 255K   |
| <i>PROCStarIII</i> 260E-2AP     | EP3SE260              | -2             | 2             | 512MB              | 4                           | 35752                           | 510K   |
| <i>PROCStarIII</i> 260E-4AP     | EP3SE260              | -2             | 4             | 1024MB             | 8                           | 71504                           | 1020K  |
| <i>PROCStarIII</i> 260E-1BP     | EP3SE260              | -3             | 1             | 256MB              | 2                           | 17876                           | 255K   |
| <i>PROCStarIII</i> 260E-2BP     | EP3SE260              | -3             | 2             | 512MB              | 4                           | 35752                           | 510K   |
| <i>PROCStarIII</i> 260E-4BP     | EP3SE260              | -3             | 4             | 1024MB             | 8                           | 71504                           | 1020K  |
| <i>PROCStarIII</i> 340L-1BP     | EPS3SL340             | -3             | 1             | 256MB              | 2                           | 20491                           | 337.5K |
| <i>PROCStarIII</i> 340L-2BP     | EPS3SL340             | -3             | 2             | 512MB              | 4                           | 40982                           | 675K   |
| <i>PROCStarIII</i> 340L-4BP     | EPS3SL340             | -3             | 4             | 1024MB             | 8                           | 81964                           | 675K   |

\* LE=Logic Element. For further information the Stratix III LEs, refer to Stratix III Device Handbook (Altera Corporation)

**Note:**

The P-power models are constructed of enlarged heat sinks and thus occupy two PCIe slots.

This chapter details the *PROCStar III* architecture and components.

## 4.1. PROCStar III Block Diagram

The *PROCStar III* system Block Diagram is shown in Figure 1.

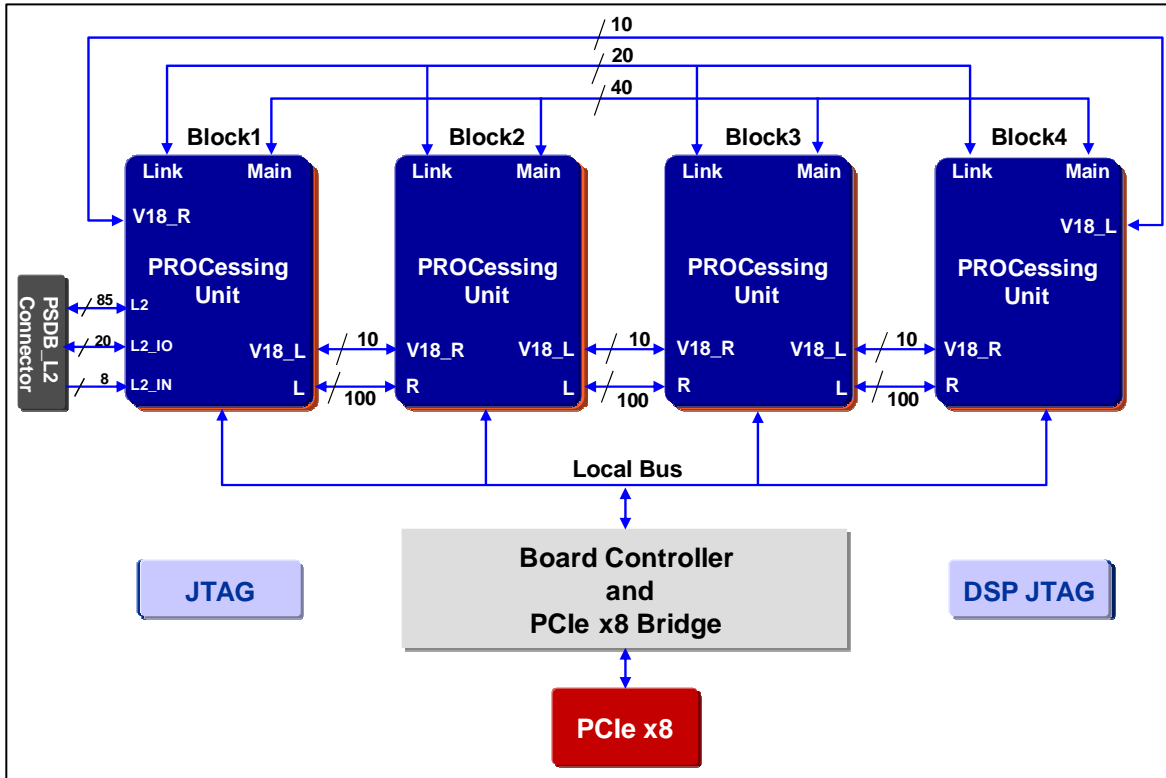


Figure 1: PROCStar III System Block Diagram

The *PROCStar III* system consists of 4 modular blocks of Processing Units. Each unit includes the following components:

- 1 ALTERA Stratix III 80E, 110E, 150L, 260E or 340L FPGAs in 1152 package.
- 256 MB DDR2 DRAM on-board memories.
- 2 x 4 GB SODIMM sockets.
- 2 PSDB (PROCStar III Daughterboard) connectors.

The *PROCStar III* Processing Unit is shown in Figure 2.

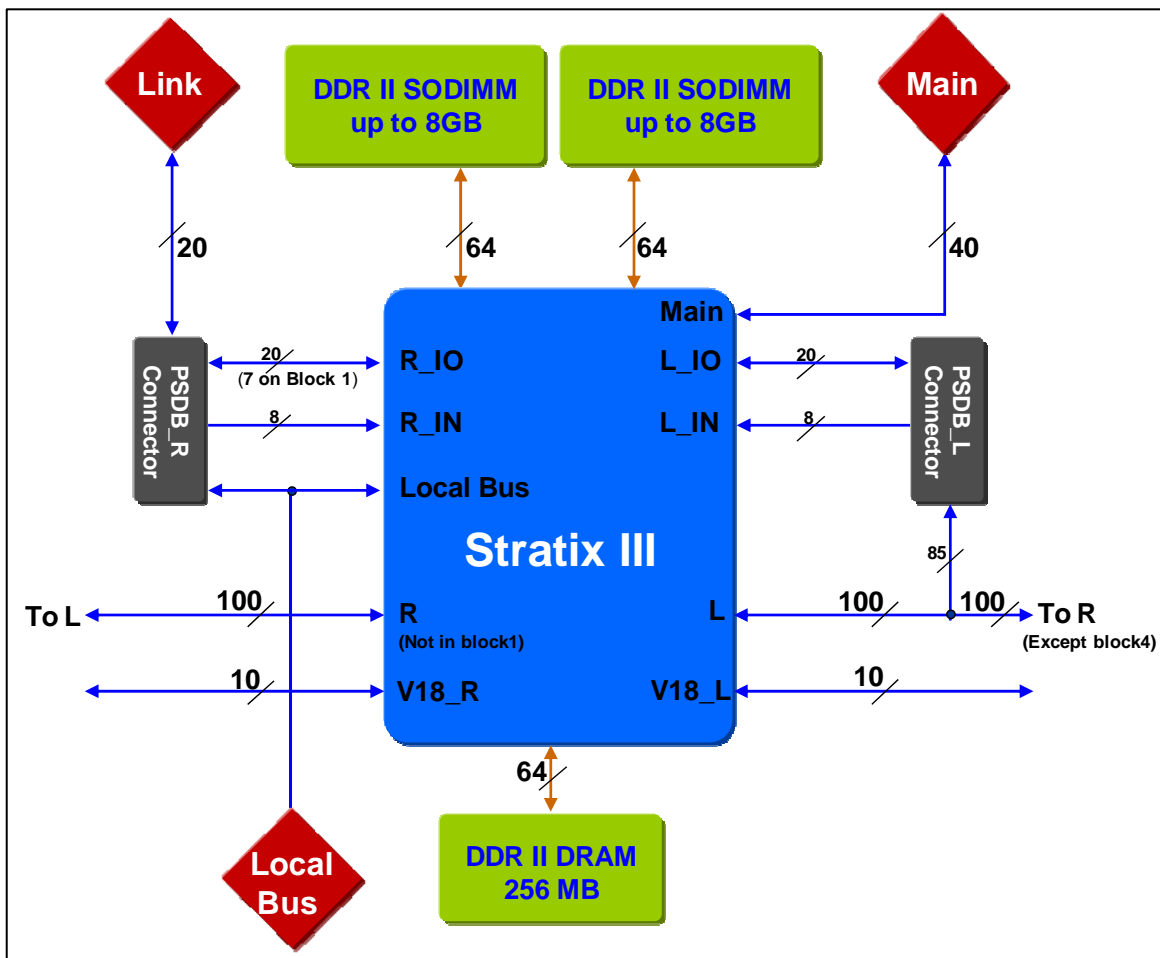


Figure 2: PROCStar III Processing Unit

The *PROCStar III* system consists of the following additional components:

- A PSDB connector connected to block 1 and block 4 with an option for LVDS interface including 24 LVDS TX , 28 LVDS RX and 2 LVDS clock inputs channels per block.
- Board controller for GiDEL's IPs and PCI Express bridge.
- 8 lane PCI Express interface

## 4.2. PROCStar III Connectivity

The *PROCStar III* connectivity is automatically generated by the *PROCWizard™* software (included in *PROC Developer's Kit*). The *PROCWizard* generates a top-level design, in Verilog, VHDL or AHDL format, including all the *PROCStar III* buses as described in the following sections. The buses will be assigned names accordingly. However, the generated names may change in the case in which a PSDB is installed on the board. In this case, buses that are connected to that PSDB will be named according to the corresponding buses on the PSDB.

|           |  |
|-----------|--|
| IMPORTANT | <p>The buses on <i>PROCStar III</i> boards were designed to provide maximum flexibility. However, user must take care to <b>avoid bus contention</b>. Always use one source at a time per signal.</p> <p>To improve EMC characteristics, it is recommended to drive each source's unused connectivity pins to "0".</p> |
|-----------|--|

### PSDB IN buses (L\_IN, R\_IN, L2\_IN)

The PSDB IN buses are dedicated input buses connecting the FPGA device to its PSDB. Inputs direction is from the PSDB to the FPGA. The L\_IN bus connects the FPGA to the left PSDB connector and the R\_IN bus connects the FPGA to the right PSDB connector. The L2\_IN bus, functionally identical to L\_IN bus, connects to the PSDB\_L2 connector as shown in Figure 1.

For further information, please refer to paragraph 6.4: *Daughterboard Connectors' Pinout*.

Each PSDB IN bus has 8 signals available to the user. Some signals are connected to dedicated clock inputs. These signals can be used as input clocks and global input lines such as clock enable.

### PSDB I/O buses (L\_IO, R\_IO, L2\_IO)

The PSDB I/O buses are I/O buses connecting an FPGA device to its PSDB. Each bus has 20 signals available to the user (only 7 signals are connected to block1 PSDB\_R). All these buses are bi-directional. The L\_IO bus connects the FPGA to the right PSDB connector and the R\_IO bus connects the FPGA to the left PSDB connector. L2\_IO bus, functionally identical to L\_IO bus, connects to the PSDB\_L2 connector as shown in Figure 1.

For further information, please refer to paragraph 6.4: Daughterboard Connectors' Pinout.

#### Note:

All the PSDB connectors have the same pin-out and mechanical dimensions. Therefore, users can choose their own PSDB location on the **PROCStar III** board. PSDB1 refers to a PSDB type 1 and uses one PSDB connector. PSDB2 refers to a PSDB type 2 and uses two PSDB connectors. For further information, refer to **PSDB1 and PSDB2 Reference Guides**.

### Link Bus

**Link bus** is a global bus connecting all PSDBs. The Link bus may be used by GiDEL PSDBs or otherwise by the user. The **Link bus** has 20 I/O signals.

### Main Bus

All Stratix III devices placed on-board are connected via the main bus. This bus has a 40 signal bus width. Two of the Main bus's lines, **main[38]** and **main[39]**, are also connected to each of the PSDB type 2 right connector on the **PROCStar III** board. For further information on PSDB type 2 (**PSDB2**), refer to the *PSDB2 Reference Guide*.

### Adjacent buses (L, R) and L2 bus

Each FPGA has two buses connected to its adjacent FPGA devices. Each Adjacent bus is 100 signal wide. The FPGAs designated names on the **PROCStar III** are **IC1**, **IC2**, **IC3** and **IC4**.

The **L bus** of each IC is connected to its right adjacent IC (i.e. IC with the preceding number) and partially (pins [84:0]) to his adjacent **PSDB\_L** connector. **L2 bus** (85 signals) is identical to **L bus** but is connected only to **PSDB\_L2** connector (only for block1).

The **R bus** of each IC is connected to the left adjacent IC (i.e. IC with the successive number).

For example, the **L bus** of IC1 is connected to its left PSDB connector and to IC2. The **R bus** of IC2 is connected to IC1.

There are two exceptions to these rules:

- IC1 has no R bus.
- IC4 L bus is not connected to IC1 (only connected to his adjacent PSDB\_L connector).

The **L[35]**, **L[38]**, **R[35]** and **R[38]** signals are connected to optional global clock input pins of the Stratix III devices. They may be used as bus clock signals.

Alternatively, the **L[35]**, **L[38]**, **R[35]** and **R[38]** signals may be used as clock inputs from PSDB to both FPGAs.

For further information, please refer to paragraph 1.1.1: *PROCStar III Individual Clocks* .

### V18 bus

The V18 bus is a 10 signals 1.8V I/O standard bus that connects between adjacent FPGA devices. The V18 bus also connect **IC4** (FPGA number 4) to **IC1**.

### Local bus

The Local bus connects all FPGAs and PSDBs to the host. An additional FPGA device placed on *PROCStar III* board implements the PCI Express Bridge, as well as DMA and PROC board controllers. The PCI Express Bridge is connected to 8-lane PCI Express bus. The **Local bus**, in turn, is connected to the PCI Express Bridge, thus connecting the host to the FPGAs and GiDEL PSDBs (only via the PSDB\_L connectors). The PCI Express Bridge is the single master of the **Local bus**.

**Note:**

*GiDEL PROCStar III* boards can act as a Master or as a Slave on the PCI Express bus. The DMA channels operate in Master mode. All the non-DMA accesses operate in the Slave mode.

*GiDEL PROCWizard* automatically generates the **Local bus** protocol within the FPGA. In addition, PROCWizard generates a simple logic bus that enables direct access to internal memory-mapped I/Os and simple interface to the internal memories. The simple bus generated by the *PROCWizard* is called the **Internal bus**.

For further information, please refer to the *PROC Internal Bus Data Book*.

**Note:**

*GiDEL* may change the **Local bus** protocol at any time without prior notice. Therefore, **Local bus** usage on the PSDB is reserved for *GiDEL*.

### 4.3. PROCStar III FPGA Identification

*PROCStar III* system includes an automatic mechanism that allows identification of the FPGA devices, the memories and the PSDBs; therefore the FPGA design can be transferred between different FPGAs with no need for recompilation.

### 4.4. PROCStar III Configurable I/O Voltage

*PROCStar III* has a dynamic I/O voltage configuration. All I/O bus voltages, except V12 local bus and memory, can be set between 2.5V to 3.0V. There are 4 configurable I/O voltages (VCCIO) in *PROCStar III*, one for each IC. The VCCIO is configured by the *PROCWizard*.

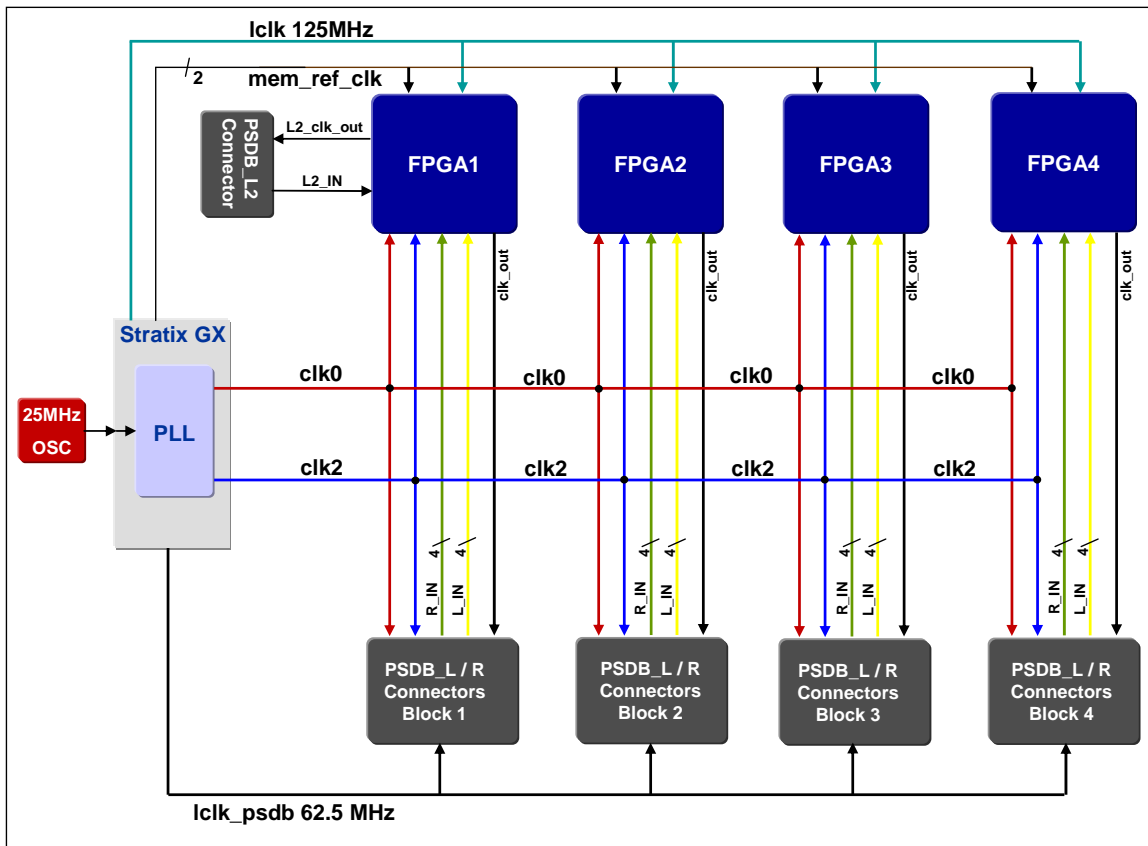
For further information, please refer to the *PROCWizard User's Manual*.

### 4.5. PROCStar III Clocking System

*GiDEL PROCStar III* boards have a flexible clocking system.

The clocks in *PROCStar III* boards are routed as shown in Figure 3:

Figure 3: PROCStar III Clock System



### 4.5.1. PROCStar III Global Clocks

#### clk0

The **clk0** is the *PROCStar III* main clock. **Clk0** drives all FPGAs and all PSDBs and is the fastest global clock. Individual clocks for user's logic can be derived from this clock in each FPGA device. *GiDEL PROCWizard* automatically generates the necessary connections to internal FPGA PLLs per FPGA for this purpose.

The **clk0** frequency can be set using the *PROCWizard*. User's software can later initialize this clock.

The **clk0** traces to the daughterboard connectors are one inch shorter than to the FPGAs. This enables the user to add daughterboard logic on the **clk0** traces and have minimal clock skew. This 1-inch trace includes the Board-to-PSDB distance (about 0.4 inch). The trace on the board should be approximately 0.6 inch to get minimal clock skew.

Within each FPGA, a PLL derives one user clock, designated **clk**. In all the FPGAs, **clk** works at the same frequency with a zero phase shift serving as a reference clock for the user's logic.

The user may set the **clk** frequency in the *PROCWizard* under *board global clocks*. For further information, refer to the *PROCWizard User Manual*.

#### Note:

1. Since the processing frequency on the Stratix III devices is very high, it is recommended that Stratix III internal clocks' frequencies, including **clk**, be an integer multiplication of the Main Clock frequency.
2. More PLLs can be added manually to derive additional internal clocks.

#### lclk

**lclk** is the **Local bus** clock. This clock drives all FPGAs and the PSDBs. Lclk frequency is 87.5MHz in the FPGA and 62.5MHz on PSDBs

#### clk2

**clk2** is an auxiliary clock that can be used as slow emulation clock. **Clk2** traces to the PSDBs are one inch shorter than to the FPGAs enabling to add daughterboard logic with minimal clock skew. The **clk2** source and frequency can be defined and set using *PROCWizard*. User's software can later initialize this clock.

## 4.5.2. PROCStar III Individual Clocks

### External clock inputs

Each FPGA has eight external clock inputs (**R\_IN[2..5]** and **L\_IN[2..5]**) from each PSDB connector, with the exception of PSDB\_L2 (**J12**). The signals are connected as shown in Table 5. PSDB\_L2 connector receives only two input clocks: **L2[35]** and **L2[38]**.

Table 5: Clock Inputs and Connections

| Clock Input               | FPGA Pin |
|---------------------------|----------|
| R_IN[2]                   | CLK10p   |
| R_IN[3]                   | CLK10n   |
| R_IN[4]                   | CLK8p    |
| R_IN[5]                   | CLK8n    |
| L_IN[2]                   | CLK1p    |
| L_IN[3]                   | CLK1n    |
| L_IN[4]                   | CLK3n    |
| L_IN[5]                   | CLK3p    |
| L2[35] (only for PSDB_L2) | CLK9p    |
| L2[38] (only for PSDB_L2) | CLK11p   |

### Adjacent Clocks

Each **Adjacent Bus** (**L** and **R**) include two signals that may be used as strobe signals for the rest of the bus. Signals **L[35]**, **L[38]** and signals **R[35]**, **R[38]** may function as bidirectional clock signals, to the left or to the right adjacent FPGA. The signals are connected as shown on Table 6.

Table 6: Adjacent Clocks

| Adjacent Clock Signal | FPGA Pin |
|-----------------------|----------|
| L[35]                 | CLK0p    |
| L[38]                 | CLK2p    |
| R[35]                 | CLK9p    |
| R[38]                 | CLK11p   |

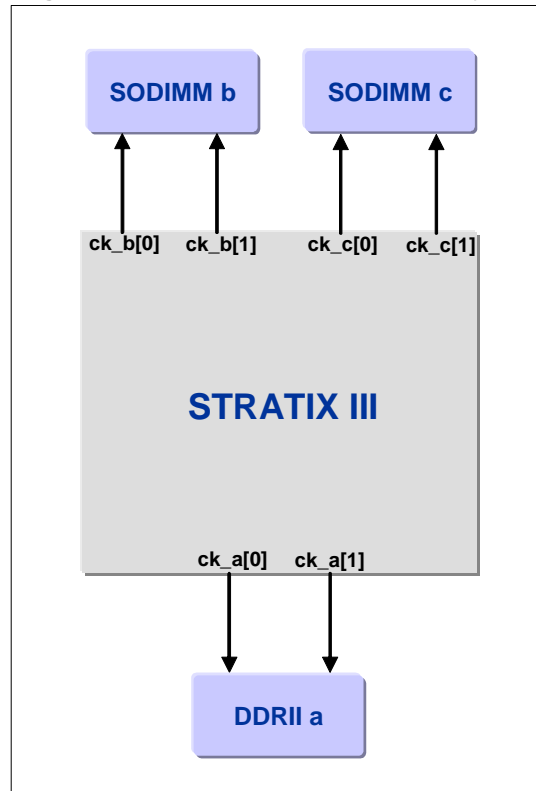
### clk\_out

There are two clock outputs, **clk\_out[1..0]**, from each on-board Stratix III device to the PSDB connectors. **clk\_out[1..0]** are connected to each Stratix III device PSDB\_L and to the PSDB\_L2.

## SODIMM and on-board Memory Clocks

Each FPGA has one on-board memory bank and two slots for DDR II SODIMMs. **PROCWizard** automatically generates the clocks to the on-board memories and to the SODIMMs connectivity as shown in Figure 4.

Figure 4: SODIMM and on-board Memory Clocks



**Note:**

All memory clocks are differential.

The SODIMM and on-board memory clocks are as follows:

Table 7: SODIMM and On-board Memory Clocks

| Clock Signal | Function                              |
|--------------|---------------------------------------|
| ck_a[0]      | on-board memory clock output (Bank A) |
| ck_a[1]      | on-board memory clock output (Bank A) |
| ck_b[0]      | SODIMM b clock output (Bank B)        |
| ck_b[1]      | SODIMM b clock output (Bank B)        |
| ck_c[0]      | SODIMM c clock output (Bank C)        |
| ck_c[1]      | SODIMM c clock output (Bank C)        |



## 5. DMA Controller

The *PROCStar III* board has up to 32 DMA channels. The DMA channels enable the board to have master control over the PCIe, while keeping simple internal logic and random access as slave only. The DMA is controlled by a driver and enables easy and effective usage of memory and system resources.

User's hardware design may control the data flow on DMA channels. For this purpose the customer should use the **user\_dreq** bus. The width of the **user\_dreq** is set according to maximum DMA channels that may be used within the design. Each bit within the bus corresponds to a specific DMA channel, so that **user\_dreq[3]**, for example, corresponds to DMA channel 3.

After the software has initialized a DMA channel, the DMA controller starts transferring data. Data continues to be transferred as long as the **user\_dreq** signal remains low for that channel. When the **user\_dreq** signal is high, the DMA controller holds the transfer. This may take up to 24 local clocks. Data transfer resumes upon asserting **user\_dreq** signal low.

**NOTE:**

1. It is not mandatory to control **user\_dreq** signals. If **user\_dreq** signals are not implemented, the DMA transfer proceeds uninterrupted. Once the DMA channel has been initialized by the software, it works continuously until all data has been transferred.
2. The DMA controller may seize and resume the DMA transfer based on the local bus, PCIe bus and system activities.

The number of enabled DMA channels is set via the *PROCWizard* as follows:


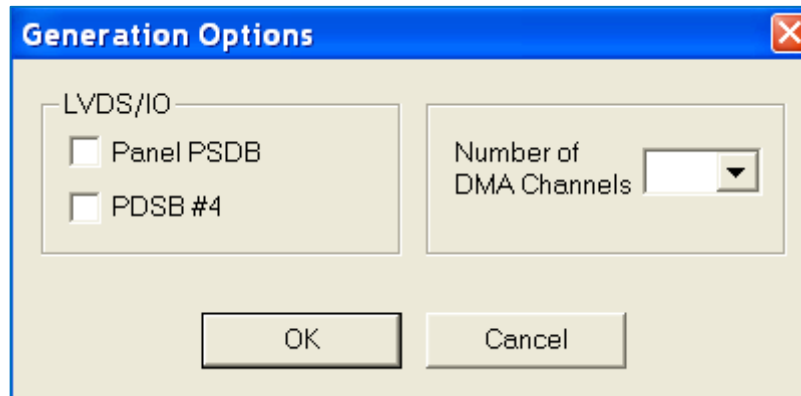
1. On the PROCWizard Toolbar select  (Configure Mode).
2. In the main window, double click the **Design Card**.
3. In the **Board Properties Dialog** box, double click **Hardware Generation Options**.
4. In the **DMA Channels** box, select the number of enabled DMA channels(see Figure 5: Selecting Number of DMA Channels).

Figure 5: Selecting Number of DMA Channels



In addition, it is possible to determine the number of enabled DMA channels using the GiDEL API, `GetDMAChannelCount()`.

For further details, refer to the *PROCWizard User's Manual* and to the *PROC API*.

## 5.1. DMA Performance

The DMA performance depends on:

- ✓ Block size
- ✓ Active PCI Express payload
- ✓ DMA method
- ✓ Host mother board and chipset

Table 9 details the DMA performance using the benchmark described in Table 8.

Table 8: DMA Performance Benchmark System

| Components                  | Specifications           |
|-----------------------------|--------------------------|
| Processor                   | Intel Pentium 4 ( 3GHz ) |
| Motherboard                 | GIGABYTE GA59SLI-S5      |
| Chipset                     | NVIDIA nForce 590        |
| Active PCI Express lanes    | 8                        |
| PCI Express payload (Bytes) | 128                      |
| DMA block size (Mega Bytes) | 8                        |
| Active DMA Channels         | 8                        |

Table 9: DMA Performance

| Test             | Results     |
|------------------|-------------|
| PC to card speed | 641 MB/Sec  |
| Card to PC Speed | 1330 MB/Sec |

This chapter details the *PROCStar III* connectors' description and pinout.

## 6.1. Connectors: Schematic Overview

Figure 6: Components Side (CS) Connectors

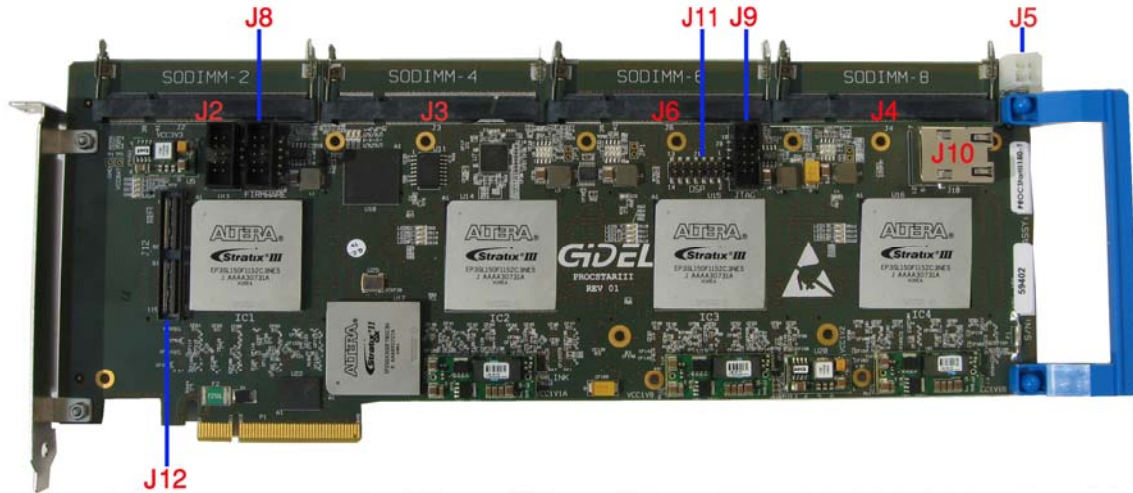
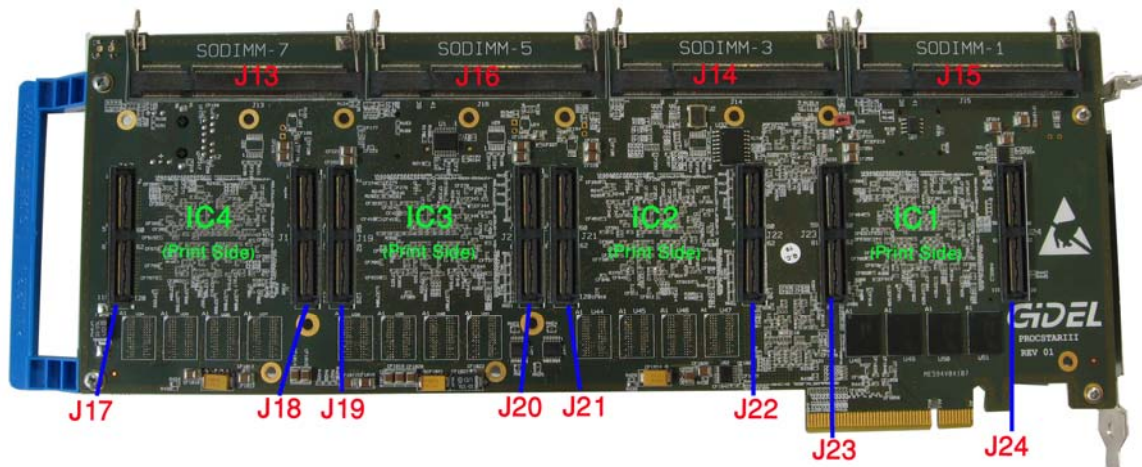


Figure 7: Print Side (PS) Connectors



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## 6.2. Daughterboard Connectors(PSDBs)

*GiDEL PROCStar III* boards may be connected to up to five daughterboards referred to as **PSDBs**. The main purpose of these daughterboards is to provide massive and fast FPGA connectivity, additional PROC boards memory storage, and unique PROC board features, such as DSPs, Camera Link, fast ADC, DAC, etc. All the PSDBs are automatically identified by the *PROCWizard*. Two kinds of daughterboards may be used: **PSDB1** (Type 1 daughterboard) and **PSDB2** (Type 2 daughterboard).

**PSDB1** use one connector each (**J17, J19, J21, J23 or J12**) in order to communicate with the *PROCStar III* board. **PSDB2** use two connectors each (**J17+J18, J19+J20, J21+J22 or J23+J24**).

**J12** and **J17** are multi-purpose connectors, and can be used also in LVDS mode.

For further information, please refer to **PSDB1 Reference Guide** and **PSDB2 Reference Guide**.

For daughterboard connectors' pinout, please refer to paragraph 6.4.

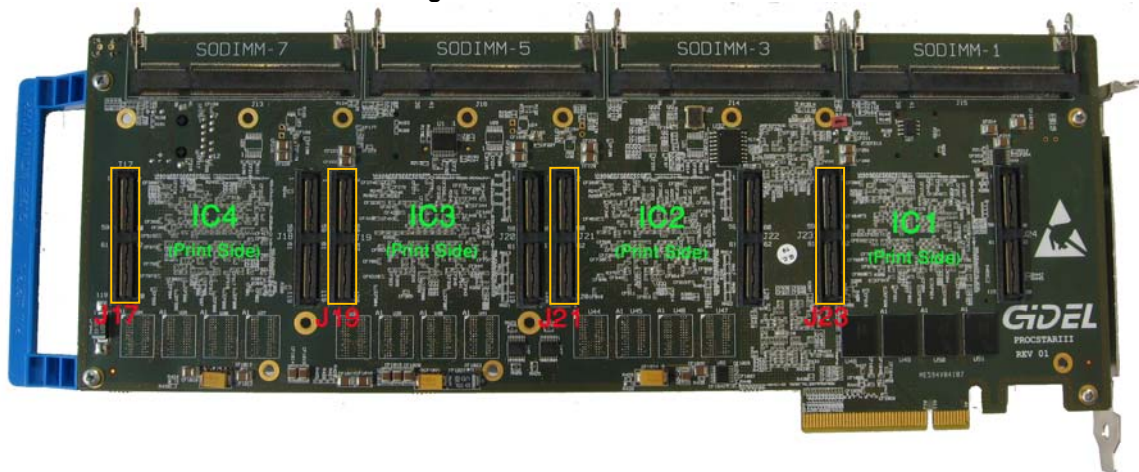
Each FPGA device has several buses that connect to the left and the right PSDB connectors referred to as **PSDB\_L** and the **PSDB\_R**. The pinouts are similar for all the corresponding connectors. This modular architecture enables the customer to use the same design within different devices or to use the same daughterboard on top of different FPGAs.

The Stratix III devices and the connectors are located on opposite side of the *PROCStar III* boards. Therefore connecting a daughterboard will not interfere with the FPGAs' cooling.

### PSDB1 Connectors (J17, J19, J21, J23 or J12)

The PSDB1 connectors, each composed of a **PSDB\_L** connector, are used to connect up to four **PSDB1** daughterboards to the **PROCStar III** board. Each **PSDB1** uses a single 120-pin connector to communicate with the **PROCStar III** board. There are four **PSDB\_L** connectors on a **PROCStar III** board's print-side available for connecting up to four **PSDB1**s as shown in Figure 8. The **PSDB1** daughterboards are secured onto the host computer's panel and use a 120-line flat cable to connect to the **PROCStar III PSDB\_L** connector. For information on flat cable types, contact the Gidel technical support.

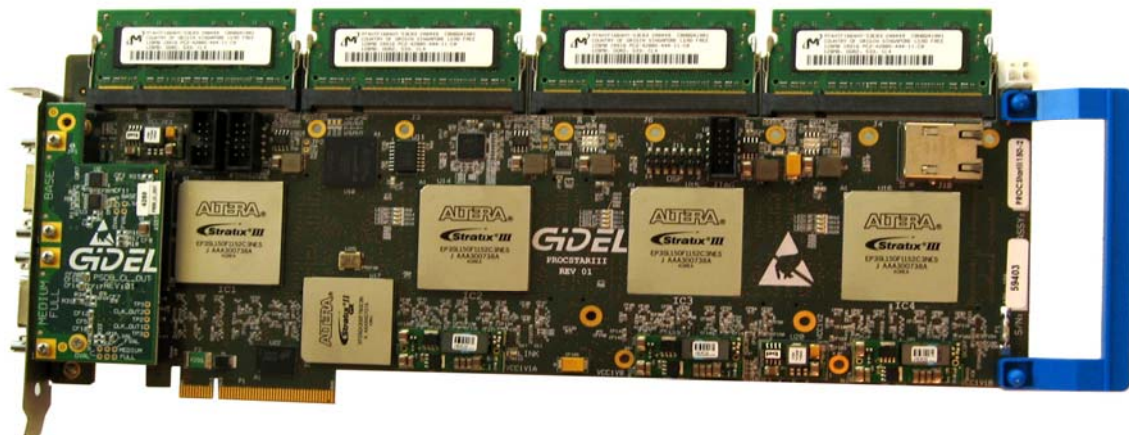
Figure 8: PSDB1 Placements



Since the FPGA devices are connected to the adjacent buses, each FPGA device may control two adjacent **PSDB1**s. For example, IC2 may control **PSDB1** on locations 2 and 3.

The **J12** connector, located on the component side, enables to mount a **PSDB1** directly on to the **PROCStar III** board as shown in Figure 9. The original **PROCStar III** metal bracket is replaced with an appropriate bracket for the daughterboard connectors.

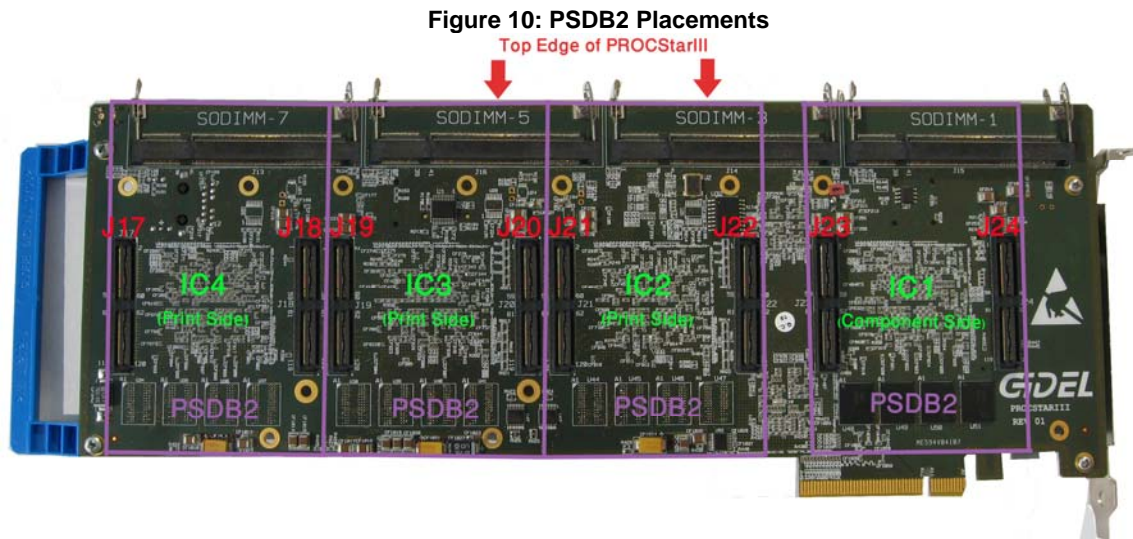
Figure 9: PSDB1 placement with external connectors



### PSDB2 Connectors (J17 & J18, J19 & J20, J21 & J22, J23 & J24)

The PSDB2 connector pairs, each composed of a **PSDB\_L** and a **PSDB\_R** connector, are used to connect up to four **PSDB2** daughterboards to the *PROCStar III* board. Each **PSDB2** uses two 120-pin connectors to communicate with the *PROCStar III* board. The main purposes of these daughterboards are to add unique functions, such as DSPs.

**PSDB2** connector pairs are located on the left and right sides of the ICs as shown in Figure 10.



When designing a **PSDB2** daughterboard, the user should orientate the PSDB2 system connectors upwards on the top-edge of the *PROCStar III* board, in order to enable a tight placement of several adjacent **PSDB2s**.

### 6.3. Dedicated Connectors

Along with the PSDB connectors, several dedicated connectors are located on the *PROCStar III* component side.

#### Dedicated connectors (J5, J8, J9, J11)

The following table details the dedicated connectors and their respective function:

Table 10: Dedicated connectors

| Connector | Function   |
|-----------|--|
| J5        | External power connector in the case of insufficient current from the PCI Express connector. |
| J8        | Firmware upgrade connector   |
| J9        | JTAG connector used for FPGA logic debug via SignalTap                                       |
| J11       | DSPs JTAG emulation connector  |

### 6.4. Daughterboard Connectors' Pinout

In the following pages, Table 11, Table 12 and Table 13 provide detailed information about the PSDB connectors (**J17 – J24** and **J12**). In addition to the information provided in the tables, note the following:

- The **R bus** of an **IC** is connected to the **L bus** of an adjacent **IC**. Therefore, signals **R(0:84)** of an IC are also connected to a PSDB mounted on adjacent IC **L(0:84)**. For example, **R(0:84)** of **IC4** is connected to **L(0:84)** of **IC3** and to **J19**.
- The **Link bus** connects all PSDBs together (except PSDB\_L2 (**J12**)).
- **J12** and **J17** are multi-purpose connectors, and can be used in LVDS mode.
- All the signals marked as **Reserved**, are reserved for GiDEL use. These pins must be disconnected at the user's PSDB

#### IMPORTANT

The bus names that appear in the tables below **may change** when a GiDEL's PSDB is installed on the *PROCStar III*. In this case, buses that are connected to that PSDB **will be named** after the corresponding buses on the PSDB.

Table 11: PSDB\_L connectors pin-out

| PSDB_L J12/J17/J19/J21/J23 |             |     |             |     |             |     |             |
|----------------------------|-------------|-----|-------------|-----|-------------|-----|-------------|
| Pin                        | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal |
| 1                          | L0          | 34  | L_IO5       | 67  | GND **      | 100 | L60         |
| 2                          | CLK_OUT1    | 35  | L24         | 68  | L_IN5       | 101 | L61         |
| 3                          | L1          | 36  | L74         | 69  | L38         | 102 | L_IO17      |
| 4                          | DB0         | 37  | L25         | 70  | L_IN4       | 103 | L62         |
| 5                          | L2          | 38  | L_IO6       | 71  | Reserved*   | 104 | L63         |
| 6                          | L_IN1       | 39  | L26         | 72  | L39         | 105 | L64         |
| 7                          | L4          | 40  | L75         | 73  | L40         | 106 | L_IO18      |
| 8                          | L3          | 41  | L27         | 74  | L_IO10      | 107 | L65         |
| 9                          | L5          | 42  | L_IO7       | 75  | L41         | 108 | L66         |
| 10                         | L_IN0       | 43  | L28         | 76  | L42         | 109 | L67         |
| 11                         | L7          | 44  | L76         | 77  | L43         | 110 | L_IO19      |
| 12                         | L6          | 45  | L29         | 78  | L_IO11      | 111 | L68         |
| 13                         | L8          | 46  | L_IO8       | 79  | L44         | 112 | L69         |
| 14                         | L_IO0       | 47  | L30         | 80  | L45         | 113 | L70         |
| 15                         | L10         | 48  | L77         | 81  | L46         | 114 | L_IN6       |
| 16                         | L9          | 49  | L31         | 82  | L_IO12      | 115 | L71         |
| 17                         | L11         | 50  | L78         | 83  | L47         | 116 | L_IN7       |
| 18                         | L_IO1       | 51  | L32         | 84  | L48         | 117 | L72         |
| 19                         | L13         | 52  | L79         | 85  | L49         | 118 | VCC 12 V    |
| 20                         | L12         | 53  | L33         | 86  | L_IO13      | 119 | L73         |
| 21                         | L14         | 54  | L80         | 87  | L50         | 120 | CLK_OUT0    |
| 22                         | L_IO2       | 55  | L34         | 88  | L51         | 121 | GND***      |
| 23                         | L16         | 56  | L_IN2       | 89  | L52         | 122 | GND***      |
| 24                         | L15         | 57  | L82         | 90  | L_IO14      | 123 | GND***      |
| 25                         | L17         | 58  | L81         | 91  | L53         | 124 | GND***      |
| 26                         | L_IO3       | 59  | L83         | 92  | L54         | 125 | VCC***      |
| 27                         | L19         | 60  | L_IN3       | 93  | L55         | 126 | VCC***      |
| 28                         | L18         | 61  | L35         | 94  | L_IO15      | 127 | VCC***      |
| 29                         | L20         | 62  | L84         | 95  | L56         | 128 | VCC***      |
| 30                         | L_IO4       | 63  | DB1         | 96  | L57         |     |             |
| 31                         | L22         | 64  | L_IO9       | 97  | L58         |     |             |
| 32                         | L21         | 65  | L36         | 98  | L_IO16      |     |             |
| 33                         | L23         | 66  | L37         | 99  | L59         |     |             |

\* Reserved for GiDEL use; must be unconnected at users PSDB.

\*\* GND pins must be connected to GND.

\*\*\* These are virtual signals. The PSDB connectors have two power strips in the middle. Signals [121..124] are connected to the top middle strip and signals [125..128] are connected to the bottom one. The top strip must be connected to GND and the bottom strip to the PSDB 3.3V source.

Table 12: PSDB\_R connectors pin-out

| PSDB_R J18/J20/J22/J24 |             |     |             |     |             |     |             |
|------------------------|-------------|-----|-------------|-----|-------------|-----|-------------|
| Pin                    | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal |
| 1                      | Reserved*   | 34  | Reserved*   | 67  | R_IO11****  | 100 | VCC 1.2V    |
| 2                      | Reserved*   | 35  | R_IN0       | 68  | Reserved*   | 101 | LINK4       |
| 3                      | Reserved*   | 36  | Reserved*   | 69  | R_IO12****  | 102 | Reserved*   |
| 4                      | Reserved*   | 37  | R_IO0       | 70  | Reserved*   | 103 | LINK5       |
| 5                      | Reserved*   | 38  | Reserved*   | 71  | R_IO13****  | 104 | VCC 1.2V    |
| 6                      | Reserved*   | 39  | R_IO1       | 72  | Reserved*   | 105 | Reserved*   |
| 7                      | LINK9       | 40  | Reserved*   | 73  | R_IO14****  | 106 | LCLK        |
| 8                      | Reserved*   | 41  | R_IO2       | 74  | Reserved*   | 107 | Reserved*   |
| 9                      | LINK10      | 42  | Reserved*   | 75  | R_IO15****  | 108 | VCC 1.2V    |
| 10                     | MAIN86      | 43  | R_IO3       | 76  | DEV_CLRN    | 109 | LINK6       |
| 11                     | LINK11      | 44  | Reserved*   | 77  | R_IO16****  | 110 | Main Clock  |
| 12                     | MAIN85      | 45  | R_IO4       | 78  | Reserved*   | 111 | LINK7       |
| 13                     | Reserved*   | 46  | Reserved*   | 79  | R_IO17****  | 112 | VCC 1.2V    |
| 14                     | Reserved*   | 47  | R_IO5       | 80  | Reserved*   | 113 | LINK8       |
| 15                     | Reserved*   | 48  | Reserved*   | 81  | R_IO18****  | 114 | CLK2        |
| 16                     | Reserved*   | 49  | R_IO6       | 82  | Reserved*   | 115 | GND **      |
| 17                     | LINK12      | 50  | Reserved*   | 83  | R_IO19****  | 116 | VCC 1.8V    |
| 18                     | Reserved*   | 51  | R_IO7****   | 84  | Reserved*   | 117 | Reserved*   |
| 19                     | LINK13      | 52  | Reserved*   | 85  | R_IN6       | 118 | Reserved*   |
| 20                     | Reserved*   | 53  | R_IO8****   | 86  | Reserved*   | 119 | Reserved*   |
| 21                     | LINK14      | 54  | Reserved*   | 87  | R_IN7       | 120 | Reserved*   |
| 22                     | Reserved*   | 55  | R_IO9****   | 88  | Reserved*   | 121 | GND***      |
| 23                     | LINK15      | 56  | Reserved*   | 89  | Reserved*   | 122 | GND***      |
| 24                     | Reserved*   | 57  | R_IN2       | 90  | Reserved*   | 123 | GND***      |
| 25                     | LINK18      | 58  | Reserved*   | 91  | LINK0       | 124 | GND***      |
| 26                     | Reserved*   | 59  | R_IN3       | 92  | VCC 1.2V    | 125 | VCC***      |
| 27                     | LINK16      | 60  | Reserved*   | 93  | LINK1       | 126 | VCC***      |
| 28                     | Reserved*   | 61  | R_IN5       | 94  | Reserved*   | 127 | VCC***      |
| 29                     | LINK17      | 62  | Reserved*   | 95  | LINK2       | 128 | VCC***      |
| 30                     | Reserved*   | 63  | R_IN4       | 96  | Reserved*   |     |             |
| 31                     | DB2         | 64  | Reserved*   | 97  | LINK19      |     |             |
| 32                     | Reserved*   | 65  | R_IO10****  | 98  | Reserved*   |     |             |
| 33                     | R_IN1       | 66  | Reserved*   | 99  | LINK3       |     |             |

\* Reserved for GiDEL use; must be unconnected at users PSDB.

\*\* GND pins must be connected to GND.

\*\*\* These are virtual signals. The PSDB connectors have two power strips in the middle. Signals [121..124] are connected to the top middle strip and signals [125..128] are connected to the bottom one. The top strip must be connected to GND and the bottom strip is the PSDB 3.3V source.

\*\*\*\* Not connected in J24 (PSDB\_R connector of IC1)

Table 13: J2 and J17 pin-out in LVDS Mode

| J12/J17 in LVDS Mode |             |     |             |     |             |     |             |
|----------------------|-------------|-----|-------------|-----|-------------|-----|-------------|
| Pin                  | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal | Pin | PSDB Signal |
| 1                    | RXp0        | 34  | TXn7        | 67  | DB2         | 100 | TXp19       |
| 2                    | TXp0        | 35  | RXn8        | 68  | NC****      | 101 | RXn23       |
| 3                    | RXn0        | 36  | TXp8        | 69  | CLK_RXp1    | 102 | TXn19       |
| 4                    | DB0         | 37  | RXp9        | 70  | NC****      | 103 | RXp24       |
| 5                    | RXp1        | 38  | TXn8        | 71  | DB3         | 104 | TXp20       |
| 6                    | TXn0        | 39  | RXn9        | 72  | TXp11       | 105 | RXn24       |
| 7                    | RXn1        | 40  | TXp9        | 73  | CLK_RXn1    | 106 | TXn20       |
| 8                    | TXp1        | 41  | RXp10       | 74  | TXn11       | 107 | RXp25       |
| 9                    | RXp2        | 42  | TXn9        | 75  | RXp17       | 108 | TXp21       |
| 10                   | TXn1        | 43  | RXn10       | 76  | TXp13       | 109 | RXn25       |
| 11                   | RXn2        | 44  | TXp10       | 77  | RXn17       | 110 | TXn21       |
| 12                   | TXp2        | 45  | RXp11       | 78  | TXn13       | 111 | RXp26       |
| 13                   | RXp3        | 46  | TXn10       | 79  | RXp18       | 112 | TXp22       |
| 14                   | TXn2        | 47  | RXn11       | 80  | TXp14       | 113 | RXn26       |
| 15                   | RXn3        | 48  | RXp13       | 81  | RXn18       | 114 | TXn22       |
| 16                   | TXp3        | 49  | RXp12       | 82  | TXn14       | 115 | RXp27       |
| 17                   | RXp4        | 50  | RXn13       | 83  | RXp19       | 116 | TXp23       |
| 18                   | TXn3        | 51  | RXn12       | 84  | TXp15       | 117 | RXn27       |
| 19                   | RXn4        | 52  | RXp14       | 85  | RXn19       | 118 | VCC12V      |
| 20                   | TXp4        | 53  | RXp15       | 86  | TXn15       | 119 | NC          |
| 21                   | RXp5        | 54  | RXn14       | 87  | RXp20       | 120 | TXn23       |
| 22                   | TXn4        | 55  | RXn15       | 88  | TXp16       | 121 | GND***      |
| 23                   | RXn5        | 56  | NC****      | 89  | RXn20       | 122 | GND***      |
| 24                   | TXp5        | 57  | RXp16       | 90  | TXn16       | 123 | GND***      |
| 25                   | RXp6        | 58  | NC****      | 91  | RXp21       | 124 | GND***      |
| 26                   | TXn5        | 59  | RXn16       | 92  | TXp17       | 125 | VCC***      |
| 27                   | RXn6        | 60  | NC****      | 93  | RXn21       | 126 | VCC***      |
| 28                   | TXp6        | 61  | CLK_RXp0    | 94  | TXn17       | 127 | VCC***      |
| 29                   | RXp7        | 62  | NC****      | 95  | RXp22       | 128 | VCC***      |
| 30                   | TXn6        | 63  | DB1         | 96  | TXp18       |     |             |
| 31                   | RXn7        | 64  | TXp12       | 97  | RXn22       |     |             |
| 32                   | TXp7        | 65  | CLK_RXn0    | 98  | TXn18       |     |             |
| 33                   | RXp8        | 66  | TXn12       | 99  | RXp23       |     |             |

\* Reserved for GiDEL use; must be unconnected at users PSDB.

\*\* GND pins must be connected to GND.

\*\*\* These are virtual signals. The PSDB connectors have two power strips in the middle. Signals [121..124] are connected to the top middle strip and signals [125..128] are connected to the bottom one. The top strip must be connected to GND and the bottom strip to the PSDB 3.3V source.

\*\*\*\* Should not be connected.

## 6.5. External Power Connector Pinout

**J5** is the external power connector. The connector pinout is described in Table 14.

Table 14: External Power Connector Pin-out

| J5 pin | Signal |
|--------|--------|
| 1      | 12V    |
| 2      | 12V    |
| 3      | GND    |
| 4      | GND    |



## 7. Memories

The *PROCStar III* system memory has a five-level structure as follows:

Three-level structure of Stratix III embedded memories:

1. **MLAB** (Memory Logic Array Blocks) 640-bit Memories
2. **M9K Blocks** 9,216-bit Memories
3. **M114K Blocks** 147,456-bit Memories

Additional two level structure of peripheral on-board memory blocks:

4. **DDRII SDRAM** 256MB 64-bit wide
5. **DDR II DRAM SODIMM** 64-bit wide

### 7.1. Three-level structure Stratix III embedded memory

The Stratix III embedded memory includes three different sizes of SRAM as described in Table 15. Each embedded memory block can be configured (depth x width), via the Quartus, to be a single-port RAM, dual-port RAM, ROM, or shift register.

Table 15 : Stratix III Embedded Memory

| Memory Type  | Memory Size | Applications  |
|--------------|-------------|---|
| MLAB         | 640-bit     | Filter delay lines, small FIFO buffers and shift registers. |
| M9K Blocks   | 9,216-bit   | General purpose memory applications.                        |
| M114K Blocks | 147,456-bit | Processor code storage, packet and video frame buffering.   |

For further information, refer to *Stratix III Device Handbook* (Altera Corporation) .

Table 16 describes the **PROCStar III** embedded memory capacity configuration respective to the amount of FPGAs devices.

Table 16: Stratix III Embedded Memory Capacity Configuration

| Device   | PROCStar III Device Capacity | Embedded Memory Capacity |            |              |                 |
|----------|------------------------------|--------------------------|------------|--------------|-----------------|
|          |                              | MLABS                    | M9K Blocks | M144K Blocks | Total RAM Kbits |
| EP3SE80  | 1                            | 1600                     | 495        | 12           | 7183            |
|          | 2                            | 3200                     | 990        | 24           | 14366           |
|          | 4                            | 6400                     | 1980       | 48           | 28732           |
| EP3SE110 | 1                            | 2150                     | 639        | 16           | 9399            |
|          | 2                            | 4300                     | 1278       | 24           | 18798           |
|          | 4                            | 8600                     | 2556       | 48           | 37596           |
| EP3SL150 | 1                            | 2850                     | 355        | 16           | 7280            |
|          | 2                            | 5700                     | 710        | 32           | 14560           |
|          | 4                            | 11400                    | 1420       | 64           | 29120           |
| EP3SE260 | 1                            | 5100                     | 864        | 48           | 17876           |
|          | 2                            | 10200                    | 1728       | 96           | 35752           |
|          | 4                            | 20400                    | 3456       | 192          | 71504           |
| EP3SL340 | 1                            | 6750                     | 1040       | 48           | 20491           |
|          | 2                            | 13500                    | 2080       | 96           | 40982           |
|          | 4                            | 27000                    | 4160       | 192          | 81964           |

## 7.2. On-board Memory Blocks - 256MB DDRII SDRAM("Block A")

Each Stratix III device has direct access to a single 64-bits wide 256 MB DDR II SDRAM memory block referred to as "**Block A**"(See Figure 2). The DDR II memory blocks may be controlled via GiDEL's innovative controller **PROCMultiPort™** or via the user's controller.

The **PROCMultiPort** conjoined with the DDR II memory block allow for acquisition, display systems and alike to function autonomously thus freeing the software from real-time response. With **PROCMultiPort**, one DDR II block may replace several external memory blocks, while enabling high throughput. Potential applications that can exploit this advantage include: huge FIFOs, on-board data processing, 3D applications, huge delay lines, virtual enlargement of Stratix III memory, simulator memory, diagnostic buffers and more.

For more information, refer to the **PROCMultiport IP User Guide**.

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### 7.3. DDR II DRAM SODIMM Modules – 64 bit wide("Block B and Block C")

For additional memory, each Stratix III device is supported by two DDR II Modules slots(200-Pin un-buffered SODIMM). Each DDR II module has a maximum capacity of 4 GB. These slots are designated "**Block B**" and "**Block C**".

The **PROCMultiPort** enables new design methodologies by replacing large and complicated designs and reducing development time. The advantages of using **PROCMultiPort** are described in paragraph 7.2 : *On-board Memory Blocks - 256MB*.

For more information on the **PROCMultiport**, refer to the **PROCMultiport IP User Guide**.

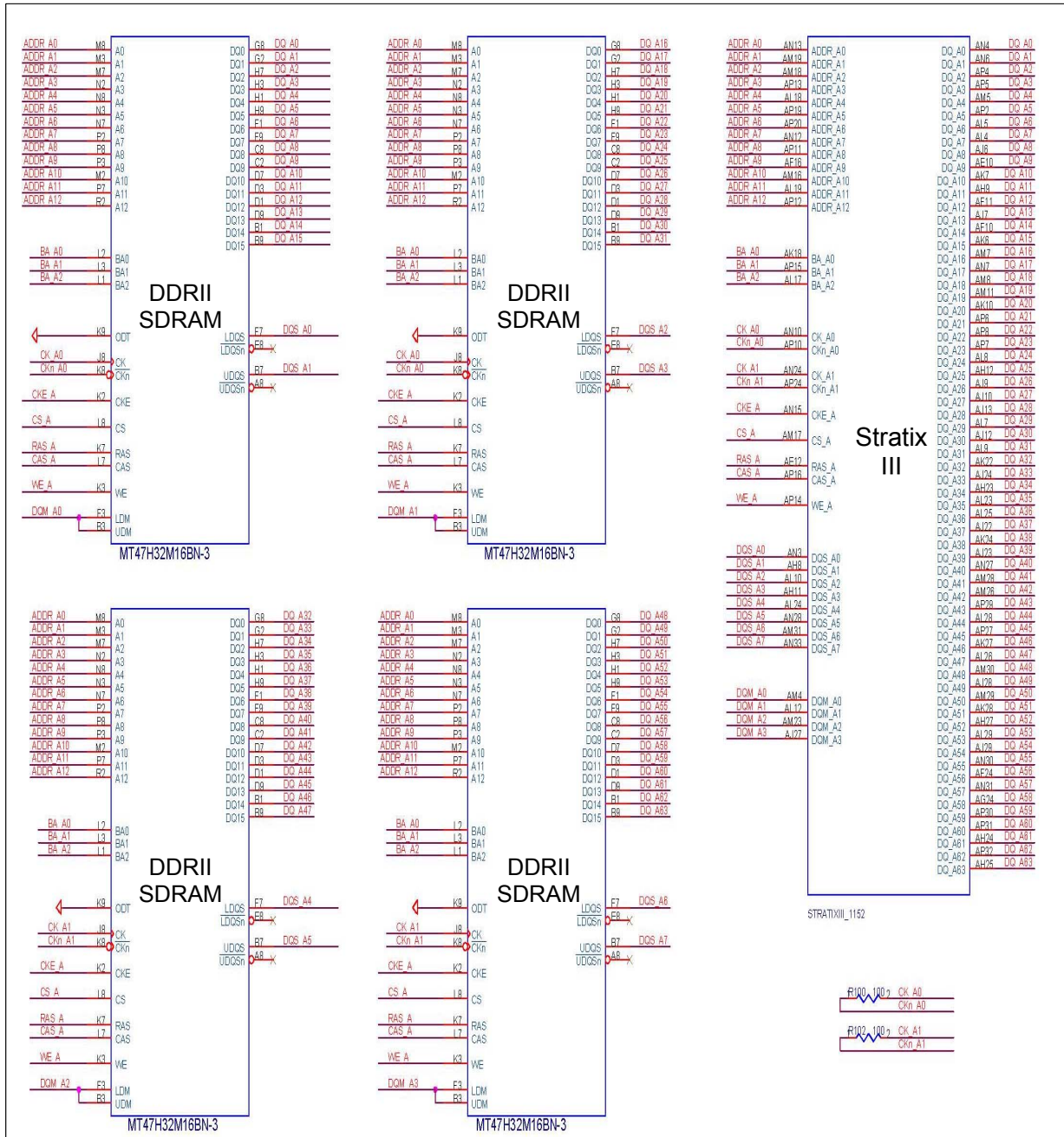
For **PROCStar III** compatible DDRII SODIMM modules please refer to the **SODIMM Type DataSheet**.document.

## 7.4. Memory Modules Pinout and Signal Connectivity

### 7.4.1. On-board DDRII SDRAM Connectivity

The following figure specifies the Stratix III and DDRII SDRAM connectivity and pinout.

Figure 11:DDR II SDRAM Connectivity and Pin-Out



### 7.4.2. DDR II DRAM SODIMM Connectivity

Figure 12 and Figure 13 show the Stratix III SODIMM memory connectivity and pinout.

Figure 12: SODIMM Bank B Connectivity and Pinout

|          |     |                |     |        |
|----------|-----|----------------|-----|--------|
| ADDR_B0  | E14 | SODIMMB ADDR0  | 102 | ADDR0  |
| ADDR_B1  | D16 | SODIMMB ADDR1  | 101 | ADDR1  |
| ADDR_B2  | H16 | SODIMMB ADDR2  | 99  | ADDR2  |
| ADDR_B3  | G17 | SODIMMB ADDR3  | 98  | ADDR3  |
| ADDR_B4  | J16 | SODIMMB ADDR4  | 98  | ADDR4  |
| ADDR_B5  | D17 | SODIMMB ADDR5  | 97  | ADDR5  |
| ADDR_B6  | F16 | SODIMMB ADDR6  | 94  | ADDR6  |
| ADDR_B7  | G16 | SODIMMB ADDR7  | 92  | ADDR7  |
| ADDR_B8  | E17 | SODIMMB ADDR8  | 93  | ADDR8  |
| ADDR_B9  | D18 | SODIMMB ADDR9  | 91  | ADDR9  |
| ADDR_B10 | C16 | SODIMMB ADDR10 | 105 | ADDR10 |
| ADDR_B11 | L19 | SODIMMB ADDR11 | 90  | ADDR11 |
| ADDR_B12 | C18 | SODIMMB ADDR12 | 89  | ADDR12 |
| ADDR_B13 | F19 | SODIMMB ADDR13 | 116 | ADDR13 |
| ADDR_B14 | K20 | SODIMMB ADDR14 | 86  | ADDR14 |
| ADDR_B15 | K17 | SODIMMB ADDR15 | 84  | ADDR15 |
| BA_B0    | E16 | SODIMMB BA0    | 107 | BA0    |
| BA_B1    | F14 | SODIMMB BA1    | 106 | BA1    |
| BA_B2    | D19 | SODIMMB BA2    | 85  | BA2    |
| DO_B0    | H34 | SODIMMB DO0    | 5   | DO0    |
| DO_B1    | G34 | SODIMMB DO1    | 7   | DO1    |
| DO_B2    | G33 | SODIMMB DO2    | 17  | DO2    |
| DO_B3    | F34 | SODIMMB DO3    | 19  | DO3    |
| DO_B4    | L31 | SODIMMB DO4    | 4   | DO4    |
| DO_B5    | L32 | SODIMMB DO5    | 6   | DO5    |
| DO_B6    | N26 | SODIMMB DO6    | 14  | DO6    |
| DO_B7    | N27 | SODIMMB DO7    | 16  | DO7    |
| DO_B8    | L29 | SODIMMB DO8    | 23  | DO8    |
| DO_B9    | K28 | SODIMMB DO9    | 25  | DO9    |
| DO_B10   | F33 | SODIMMB DO10   | 35  | DO10   |
| DO_B11   | E34 | SODIMMB DO11   | 37  | DO11   |
| DO_B12   | K30 | SODIMMB DO12   | 22  | DO12   |
| DO_B13   | M27 | SODIMMB DO13   | 22  | DO13   |
| DO_B14   | D34 | SODIMMB DO14   | 36  | DO14   |
| DO_B15   | D33 | SODIMMB DO15   | 38  | DO15   |
| DO_B16   | J29 | SODIMMB DO16   | 43  | DO16   |
| DO_B17   | J30 | SODIMMB DO17   | 45  | DO17   |
| DO_B18   | K27 | SODIMMB DO18   | 55  | DO18   |
| DO_B19   | N25 | SODIMMB DO19   | 57  | DO19   |
| DO_B20   | H31 | SODIMMB DO20   | 44  | DO20   |
| DO_B21   | F31 | SODIMMB DO21   | 46  | DO21   |
| DO_B22   | F32 | SODIMMB DO22   | 46  | DO22   |
| DO_B23   | K28 | SODIMMB DO23   | 58  | DO23   |
| DO_B24   | A29 | SODIMMB DO24   | 61  | DO24   |
| DO_B25   | A28 | SODIMMB DO25   | 63  | DO25   |
| DO_B26   | C24 | SODIMMB DO26   | 73  | DO26   |
| DO_B27   | B28 | SODIMMB DO27   | 75  | DO27   |
| DO_B28   | C27 | SODIMMB DO28   | 62  | DO28   |
| DO_B29   | C28 | SODIMMB DO29   | 74  | DO29   |
| DO_B30   | D25 | SODIMMB DO30   | 74  | DO30   |
| DO_B31   | D24 | SODIMMB DO31   | 76  | DO31   |
| DO_B32   | J21 | SODIMMB DO32   | 123 | DO32   |
| DO_B33   | K21 | SODIMMB DO33   | 125 | DO33   |
| DO_B34   | K22 | SODIMMB DO34   | 135 | DO34   |
| DO_B35   | J22 | SODIMMB DO35   | 137 | DO35   |
| DO_B36   | J20 | SODIMMB DO36   | 124 | DO36   |
| DO_B37   | A24 | SODIMMB DO37   | 126 | DO37   |
| DO_B38   | B25 | SODIMMB DO38   | 134 | DO38   |
| DO_B39   | A26 | SODIMMB DO39   | 136 | DO39   |
| DO_B40   | A6  | SODIMMB DO40   | 141 | DO40   |
| DO_B41   | D8  | SODIMMB DO41   | 143 | DO41   |
| DO_B42   | E8  | SODIMMB DO42   | 151 | DO42   |
| DO_B43   | D7  | SODIMMB DO43   | 153 | DO43   |
| DO_B44   | C9  | SODIMMB DO44   | 140 | DO44   |
| DO_B45   | D9  | SODIMMB DO45   | 142 | DO45   |
| DO_B46   | A8  | SODIMMB DO46   | 152 | DO46   |
| DO_B47   | B8  | SODIMMB DO47   | 154 | DO47   |
| DO_B48   | C6  | SODIMMB DO48   | 157 | DO48   |
| DO_B49   | B5  | SODIMMB DO49   | 159 | DO49   |
| DO_B50   | C5  | SODIMMB DO50   | 173 | DO50   |
| DO_B51   | D6  | SODIMMB DO51   | 175 | DO51   |
| DO_B52   | G8  | SODIMMB DO52   | 158 | DO52   |
| DO_B53   | E7  | SODIMMB DO53   | 160 | DO53   |
| DO_B54   | F7  | SODIMMB DO54   | 174 | DO54   |
| DO_B55   | F6  | SODIMMB DO55   | 176 | DO55   |
| DO_B56   | G11 | SODIMMB DO56   | 179 | DO56   |
| DO_B57   | G9  | SODIMMB DO57   | 181 | DO57   |
| DO_B58   | H11 | SODIMMB DO58   | 189 | DO58   |
| DO_B59   | J11 | SODIMMB DO59   | 191 | DO59   |
| DO_B60   | A4  | SODIMMB DO60   | 180 | DO60   |
| DO_B61   | A5  | SODIMMB DO61   | 182 | DO61   |
| DO_B62   | A3  | SODIMMB DO62   | 194 | DO62   |
| DO_B63   | B4  | SODIMMB DO63   | 194 | DO63   |
| RAS_B    | E13 | SODIMMB RAS    | 108 | RAS    |
| CAS_B    | D15 | SODIMMB CAS    | 113 | CAS    |
| WE_B     | C15 | SODIMMB WE     | 109 | WE     |
| CK_B0    | K33 | SODIMMB CK0    | 30  | CK0    |
| CKn_B0   | K34 | SODIMMB CKN0   | 32  | CK0#   |
| CKn_B1   | H2  | SODIMMB CK1    | 164 | CK1#   |
| CKn_B1   | J1  | SODIMMB CK1#   | 166 | CK1    |
| CKE_B0   | C19 | SODIMMB CKE0   | 79  | CKE0   |
| CKE_B1   | F20 | SODIMMB CKE1   | 80  | CKE1   |
| CS_B0    | G13 | SODIMMB CS0    | 110 | S0     |
| CS_B1    | C14 | SODIMMB CS1    | 115 | S1     |
| DQM_B0   | M28 | SODIMMB DM0    | 10  | DM0    |
| DQM_B1   | L28 | SODIMMB DM1    | 26  | DM1    |
| DQM_B2   | H32 | SODIMMB DM2    | 52  | DM2    |
| DQM_B3   | A27 | SODIMMB DM3    | 57  | DM3    |
| DQM_B4   | A25 | SODIMMB DM4    | 130 | DM4    |
| DQM_B5   | C7  | SODIMMB DM5    | 147 | DM5    |
| DQM_B6   | F8  | SODIMMB DM6    | 170 | DM6    |
| DQM_B7   | G10 | SODIMMB DM7    | 185 | DM7    |
| DQS_B0   | K31 | SODIMMB DQS0   | 13  | DQS0   |
| DQS_B1   | J31 | SODIMMB DQS1   | 31  | DQS1   |
| DQS_B2   | G33 | SODIMMB DQS2   | 51  | DQS2   |
| DQS_B3   | E23 | SODIMMB DQS3   | 70  | DQS3   |
| DQS_B4   | C26 | SODIMMB DQS4   | 131 | DQS4   |
| DQS_B5   | E7  | SODIMMB DQS5   | 148 | DQS5   |
| DQS_B6   | C4  | SODIMMB DQS6   | 169 | DQS6   |
| DQS_B7   | B2  | SODIMMB DQS7   | 188 | DQS7   |
| DQSn_B0  | K32 | SODIMMB DQSn0  | 11  | DQS0#  |
| DQSn_B1  | J32 | SODIMMB DQSn1  | 29  | DQS1#  |
| DQSn_B2  | C34 | SODIMMB DQSn2  | 49  | DQS2#  |
| DQSn_B3  | D23 | SODIMMB DQSn3  | 68  | DQS3#  |
| DQSn_B4  | B26 | SODIMMB DQSn4  | 129 | DQS4#  |
| DQSn_B5  | A7  | SODIMMB DQSn5  | 146 | DQS5#  |
| DQSn_B6  | C3  | SODIMMB DQSn6  | 167 | DQS6#  |
| DQSn_B7  | A2  | SODIMMB DQSn7  | 186 | DQS7#  |
| SCL_B    | C23 | SODIMM SCL     | 197 | SCL    |
| SDA_B    | C21 | SODIMM SDA     | 195 | SDA    |
|          |     | SA = 00        | 198 | SA0    |
|          |     |                | 200 | SA1    |
| ODT_B0   | E10 | SODIMMB ODT0   | 114 | ODT0   |
| ODT_B1   | D14 | SODIMMB ODT1   | 119 | ODT1   |

ALTERA  
STRATIX III

SODIMM-200 CONNECTOR

Figure 13: SODIMM Bank C Connectivity and Pinout

|          |     |                |     |        |
|----------|-----|----------------|-----|--------|
| ADDR_C0  | L20 | SODIMMT_ADDR0  | 102 | ADDR0  |
| ADDR_C1  | A19 | SODIMMT_ADDR1  | 101 | ADDR1  |
| ADDR_C2  | H20 | SODIMMT_ADDR2  | 100 | ADDR2  |
| ADDR_C3  | A17 | SODIMMT_ADDR3  | 99  | ADDR3  |
| ADDR_C4  | J19 | SODIMMT_ADDR4  | 98  | ADDR4  |
| ADDR_C5  | A16 | SODIMMT_ADDR5  | 97  | ADDR5  |
| ADDR_C6  | L17 | SODIMMT_ADDR6  | 94  | ADDR6  |
| ADDR_C7  | F15 | SODIMMT_ADDR7  | 92  | ADDR7  |
| ADDR_C8  | A15 | SODIMMT_ADDR8  | 93  | ADDR8  |
| ADDR_C9  | A54 | SODIMMT_ADDR9  | 91  | ADDR9  |
| ADDR_C10 | A20 | SODIMMT_ADDR10 | 105 | ADDR10 |
| ADDR_C11 | K16 | SODIMMT_ADDR11 | 90  | ADDR11 |
| ADDR_C12 | B14 | SODIMMT_ADDR12 | 89  | ADDR12 |
| ADDR_C13 | B23 | SODIMMT_ADDR13 | 116 | ADDR13 |
| ADDR_C14 | J15 | SODIMMT_ADDR14 | 86  | ADDR14 |
| ADDR_C15 | L16 | SODIMMT_ADDR15 | 84  | ADDR15 |
| BA_C0    | B20 | SODIMMT_BA0    | 107 | BA0    |
| BA_C1    | K19 | SODIMMT_BA1    | 106 | BA1    |
| BA_C2    | A13 | SODIMMT_BA2    | 85  | BA2    |
| DQ_C0    | L5  | SODIMMT_DQ0    | 5   | DQ0    |
| DQ_C1    | N8  | SODIMMT_DQ1    | 7   | DQ1    |
| DQ_C2    | L6  | SODIMMT_DQ2    | 17  | DQ2    |
| DQ_C3    | L7  | SODIMMT_DQ3    | 19  | DQ3    |
| DQ_C4    | L4  | SODIMMT_DQ4    | 4   | DQ4    |
| DQ_C5    | G1  | SODIMMT_DQ5    | 6   | DQ5    |
| DQ_C6    | F1  | SODIMMT_DQ6    | 14  | DQ6    |
| DQ_C7    | G2  | SODIMMT_DQ7    | 16  | DQ7    |
| DQ_C8    | N10 | SODIMMT_DQ8    | 23  | DQ8    |
| DQ_C9    | K5  | SODIMMT_DQ9    | 25  | DQ9    |
| DQ_C10   | K6  | SODIMMT_DQ10   | 35  | DQ10   |
| DQ_C11   | H3  | SODIMMT_DQ11   | 37  | DQ11   |
| DQ_C12   | J6  | SODIMMT_DQ12   | 20  | DQ12   |
| DQ_C13   | H4  | SODIMMT_DQ13   | 22  | DQ13   |
| DQ_C14   | F3  | SODIMMT_DQ14   | 36  | DQ14   |
| DQ_C15   | J7  | SODIMMT_DQ15   | 38  | DQ15   |
| DQ_C16   | L8  | SODIMMT_DQ16   | 43  | DQ16   |
| DQ_C17   | K7  | SODIMMT_DQ17   | 45  | DQ17   |
| DQ_C18   | M9  | SODIMMT_DQ18   | 55  | DQ18   |
| DQ_C19   | L9  | SODIMMT_DQ19   | 57  | DQ19   |
| DQ_C20   | D2  | SODIMMT_DQ20   | 44  | DQ20   |
| DQ_C21   | G4  | SODIMMT_DQ21   | 46  | DQ21   |
| DQ_C22   | G5  | SODIMMT_DQ22   | 56  | DQ22   |
| DQ_C23   | K8  | SODIMMT_DQ23   | 58  | DQ23   |
| DQ_C24   | A9  | SODIMMT_DQ24   | 61  | DQ24   |
| DQ_C25   | B11 | SODIMMT_DQ25   | 63  | DQ25   |
| DQ_C26   | A12 | SODIMMT_DQ26   | 73  | DQ26   |
| DQ_C27   | L14 | SODIMMT_DQ27   | 75  | DQ27   |
| DQ_C28   | K13 | SODIMMT_DQ28   | 62  | DQ28   |
| DQ_C29   | K14 | SODIMMT_DQ29   | 64  | DQ29   |
| DQ_C30   | J14 | SODIMMT_DQ30   | 74  | DQ30   |
| DQ_C31   | H14 | SODIMMT_DQ31   | 76  | DQ31   |
| DQ_C32   | F13 | SODIMMT_DQ32   | 123 | DQ32   |
| DQ_C33   | F12 | SODIMMT_DQ33   | 125 | DQ33   |
| DQ_C34   | G12 | SODIMMT_DQ34   | 135 | DQ34   |
| DQ_C35   | F11 | SODIMMT_DQ35   | 137 | DQ35   |
| DQ_C36   | C12 | SODIMMT_DQ36   | 124 | DQ36   |
| DQ_C37   | D12 | SODIMMT_DQ37   | 126 | DQ37   |
| DQ_C38   | D10 | SODIMMT_DQ38   | 134 | DQ38   |
| DQ_C39   | E11 | SODIMMT_DQ39   | 136 | DQ39   |
| DQ_C40   | G23 | SODIMMT_DQ40   | 141 | DQ40   |
| DQ_C41   | F23 | SODIMMT_DQ41   | 143 | DQ41   |
| DQ_C42   | F26 | SODIMMT_DQ42   | 151 | DQ42   |
| DQ_C43   | E26 | SODIMMT_DQ43   | 153 | DQ43   |
| DQ_C44   | F22 | SODIMMT_DQ44   | 140 | DQ44   |
| DQ_C45   | D26 | SODIMMT_DQ45   | 142 | DQ45   |
| DQ_C46   | D27 | SODIMMT_DQ46   | 152 | DQ46   |
| DQ_C47   | D28 | SODIMMT_DQ47   | 154 | DQ47   |
| DQ_C48   | K25 | SODIMMT_DQ48   | 157 | DQ48   |
| DQ_C49   | G26 | SODIMMT_DQ49   | 159 | DQ49   |
| DQ_C50   | E28 | SODIMMT_DQ50   | 173 | DQ50   |
| DQ_C51   | F28 | SODIMMT_DQ51   | 175 | DQ51   |
| DQ_C52   | J24 | SODIMMT_DQ52   | 158 | DQ52   |
| DQ_C53   | J25 | SODIMMT_DQ53   | 160 | DQ53   |
| DQ_C54   | G27 | SODIMMT_DQ54   | 174 | DQ54   |
| DQ_C55   | F27 | SODIMMT_DQ55   | 176 | DQ55   |
| DQ_C56   | B29 | SODIMMT_DQ56   | 179 | DQ56   |
| DQ_C57   | A30 | SODIMMT_DQ57   | 181 | DQ57   |
| DQ_C58   | B31 | SODIMMT_DQ58   | 189 | DQ58   |
| DQ_C59   | C31 | SODIMMT_DQ59   | 191 | DQ59   |
| DQ_C60   | C29 | SODIMMT_DQ60   | 180 | DQ60   |
| DQ_C61   | C30 | SODIMMT_DQ61   | 182 | DQ61   |
| DQ_C62   | D31 | SODIMMT_DQ62   | 192 | DQ62   |
| DQ_C63   | A33 | SODIMMT_DQ63   | 194 | DQ63   |
| RAS_C    | F19 | SODIMMT_RAS    | 108 | RAS    |
| CAS_C    | A22 | SODIMMT_CAS    | 113 | CAS    |
| WE_C     | A21 | SODIMMT_WE     | 109 | WE     |
| CK_C0    | E4  | SODIMMT_CK0    | 30  | CK0    |
| CKn_C0   | E3  | SODIMMT_CK0#   | 32  | CK0#   |
| CK_C1    | J33 | SODIMMT_CK1    | 164 | CK1    |
| CKn_C1   | J34 | SODIMMT_CK1#   | 166 | CK1#   |
| CKE_C0   | B13 | SODIMMT_CKE0   | 79  | CKE0   |
| CKE_C1   | K15 | SODIMMT_CKE1   | 80  | CKE1   |
| CS_C0    | G20 | SODIMMT_CS0    | 110 | S0     |
| CS_C1    | B22 | SODIMMT_CS1    | 115 | S1     |
| DQM_C0   | H1  | SODIMMT_DM0    | 10  | DM0    |
| DQM_C1   | F4  | SODIMMT_DM1    | 26  | DM1    |
| DQM_C2   | D3  | SODIMMT_DM2    | 52  | DM2    |
| DQM_C3   | A11 | SODIMMT_DM3    | 67  | DM3    |
| DQM_C4   | D13 | SODIMMT_DM4    | 130 | DM4    |
| DQM_C5   | F25 | SODIMMT_DM5    | 147 | DM5    |
| DQM_C6   | H26 | SODIMMT_DM6    | 170 | DM6    |
| DQM_C7   | A31 | SODIMMT_DM7    | 185 | DM7    |
| DQS_C0   | J4  | SODIMMT_DS0    | 13  | DQS0   |
| DQS_C1   | E2  | SODIMMT_DS1    | 31  | DQS1   |
| DQS_C2   | C1  | SODIMMT_DS2    | 51  | DQS2   |
| DQS_C3   | B10 | SODIMMT_DS3    | 70  | DQS3   |
| DQS_C4   | D11 | SODIMMT_DS4    | 131 | DQS4   |
| DQS_C5   | G24 | SODIMMT_DS5    | 148 | DQS5   |
| DQS_C6   | F29 | SODIMMT_DS6    | 169 | DQS6   |
| DQS_C7   | B32 | SODIMMT_DS7    | 186 | DQS7   |
| DQSn_C0  | J3  | SODIMMT_DS0#   | 11  | DQS0#  |
| DQSn_C1  | E1  | SODIMMT_DS1#   | 29  | DQS1#  |
| DQSn_C2  | D1  | SODIMMT_DS2#   | 49  | DQS2#  |
| DQSn_C3  | A10 | SODIMMT_DS3#   | 68  | DQS3#  |
| DQSn_C4  | C11 | SODIMMT_DS4#   | 129 | DQS4#  |
| DQSn_C5  | F24 | SODIMMT_DS5#   | 146 | DQS5#  |
| DQSn_C6  | E29 | SODIMMT_DS6#   | 167 | DQS6#  |
| DQSn_C7  | A32 | SODIMMT_DS7#   | 186 | DQS7#  |
| SCL_C    | J12 | SODIMM_SCL     | 197 | SCL    |
| SDA_C    | C20 | SODIMM_SDA     | 195 | SDA    |
|          |     | SA = 01        | 198 | SA0    |
|          |     |                | 200 | SA1    |
| ODT_C0   | E19 | SODIMMT_ODT0   | 114 | ODT0   |
| ODT_C1   | A23 | SODIMMT_ODT1   | 119 | ODT1   |

ALTERA  
STRATIX III

SODIMM-200 CONNECTOR



## 8. LEDs

### 8.1. Power LEDs

A 3.3V power LED is located on the upper side of the *PROCStar III* boards.

An illuminated power LED indicates that the board is receiving power from the PCI / external source.

### 8.2. Status LEDs

The *PROCStar III* board has four status LEDs:

Table 17: Status LEDs

| LED      | Function   |
|----------|--|
| LINK Led | Indicates that the board has established link with PCI express slot  |
| STSLED0  | Temperature indicator:<br><b>Blinking</b> : temperature approaching to critical level<br><b>Constant on</b> : over-temperature |
| STSLED1  | Blinking to indicate that card is operational  |
| STSLED2  | Reserved   |

### 8.3. User's LEDs

*PROCStar III* boards contain 4 user's LEDs connected to each Stratix III device through R\_IO bus as described on Table 18.

Table 18: User's LEDs

| LED   | Stratix device ID |
|-------|-------------------|
| LED 1 | R_IO0             |
| LED 2 | R_IO1             |
| LED 3 | R_IO2             |
| LED 4 | R_IO3             |



## 9. Technical Specifications

### 9.1. Electrical and Mechanical Environment

#### 9.1.1. Humidity

The *PROCStar III* is operational under the following humidity conditions:

Humidity: 10 - 90% (non-condensing)

#### 9.1.2. Temperature

The *PROCStar III* board is equipped with an on-board temperature controller. If an FPGA overheats, all FPGAs are automatically unloaded to protect the board.

The *PROCStar III* operating limits depend on the IC type, the computer ambient temperature, and the computer air flow as detailed in the following table:

Figure 14: PROCStar III Operating Conditions

| IC Type | Max Power consumption per IC[W] | Max.Computer Ambient Temp | Min Computer Air Flow [m/sec] |
|---------|---------------------------------|---------------------------|-------------------------------|
| All     | 8.5                             | 40                        | 2.5                           |
|         | 10.4                            | 35                        | 2.5                           |
|         | 10.4                            | 45                        | 4                             |
|         | 17*                             | 30                        | 4                             |
| 260**   | 17*                             | 40                        | 3                             |
| 340**   | 21                              | 30                        | 3                             |

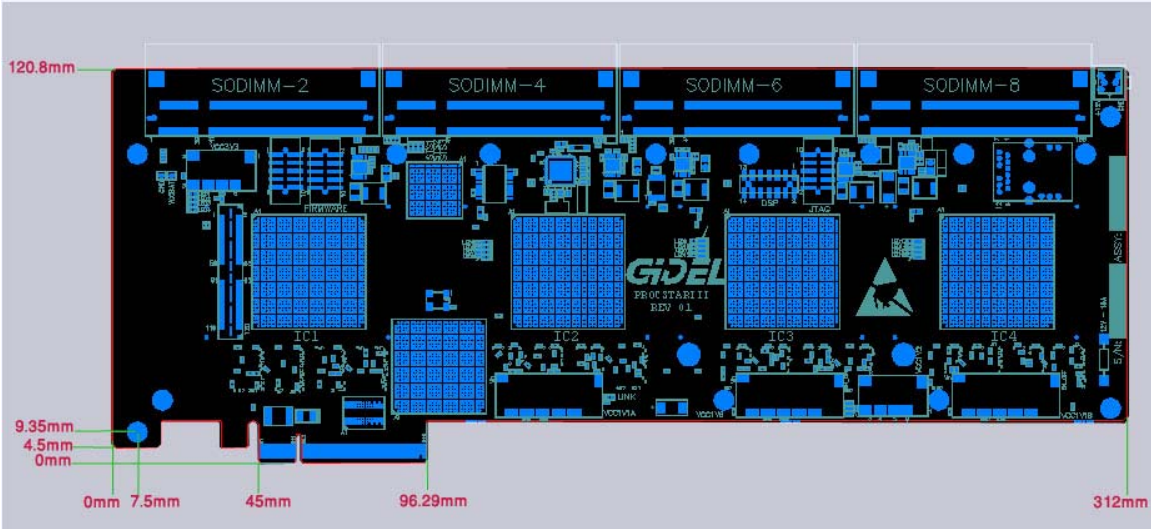
\*17 W per IC but up to 29 W per IC couples: IC1+IC2 or IC3+IC4

\*\* High-power **P** models

## 9.2. PROCStar III Mechanical Description

PROCStar III mechanical dimensions, as shown in Figure 15, comply with PCI Express mechanical standards with the exception of the board height and the SODIMMs and the PSDB connector dimensions.

Figure 15: PROCStar III Mechanical Dimensions



For PROCStar III daughterboard mechanical dimensions, please refer to the specific PSDB1 and PSDB2 Data Book.

## 9.3. Power Consumption

PROCStar III is powered by 12V, supplied either by the PCI Express slot or by an external power supply. The maximum allowable currents are summarized in the following table:

Table 19: Maximum current Limits

| Source    | Max Current |
|-----------|-------------|
| External  | 15A         |
| PCIe Slot | 2.1A        |

The following table summarizes the *PROCStar III* internal voltage sources:

Table 20: PROCStar III internal voltage Sources

| Voltage | Description                   | Max Allowable Current | Typical Current   |
|---------|-------------------------------|-----------------------|-------------------|
| VCCCORE | Stratix III 1.1V core voltage | 20A for (IC1 + IC2)   | (1)               |
|         |                               | 20A for (IC3 + IC4)   |                   |
| VCCMEM  | 1.8V DDRII SDRAM power supply | 16A                   | (2)               |
| VCCIO   | 3.0/2.5V I/O power supply     | 3A per IC             | 1A <sup>(3)</sup> |

- (1) The VCCCORE current consumption depends on the FPGA logic usage and on the system frequency. For precise power consumption information, refer to Quartus power analyzer report.
- (2) The VCCMEM current can be calculated by the following formula:

$$I_{(VCCMEM)} = 0.4A + I_{(SODIMM\_A)} + I_{(SODIMM\_B)}$$

Where  $I_{SODIMM\_A}$  and  $I_{SODIMM\_B}$  are the currents supplied to each of the SODIMMs . The current values depend on the SODIMM capacity and the sustain rate. For more information on the SODIMM, refer to the SODIMM data sheet.

- (3) The VCCIO supplies power to all the I/O busses, except for the memory and local busses. The power consumption is dependent on I/O frequency and toggle rate. For precise power consumption information, refer to Quartus power analyzer report.

The following table summarizes the **PROCStar III** power sources supplied to the PSDBs.

Table 21: PSDB Power Sources

| Voltage   | Max Allowable Current<br>(For all PSDBs) | Max Allowable current per PSDB | Target |       |
|-----------|--|--------------------------------|--------|-------|
|           |  |                                | PSDB1  | PSDB2 |
| PSDB_3.3V | 5A                                       | 3A                             | √      | √     |
| PSDB_12V  | (1)                                      | 1A                             | √      | √     |
| PSDB_1.8V | (2)                                      | 1A                             | -      | √     |
| PSDB_1.2V | 2A                                       | 2A                             | -      | √     |

(1) The power capacity of the PCIe slot or the 12 V external power source defines the maximum allowable current that can be supplied to the PSDBs. Use the power consumption formulas provided below to insure that power capacity is not exceeded.

(2) The 1.8V power supplied to PSDBs is limited by the onboard DC-DC converter.

The sum of  $I_{(VCCMEM)}$  and PSDB\_1.8V current must exceed 16A.

Total power consumption of PROCStar III can be calculated according to the following formulas:

$$P_{TOTAL} = 1.0W + P_{PSDB} + P_{BOARD}$$

$$P_{BOARD} = 1.8V \times I_{VCCMEM} + 3.0V \times I_{VCCIO} + 1.1V \times I_{VCCCORE}$$

$$P_{PSDB} = 1.8V \times I_{PSDB_1.8} + 3.3V \times I_{PSDB_3.3V} + 12V \times I_{PSDB_12V} + 1.2V \times I_{PSDB_12V}$$

The 12V source total current can be calculated according to the following formula and must not exceed values specified in Table 19.

$$I_{12V} = P_{TOTAL} / 12V$$

## 9.4. PROCStar III Timing Model

### 9.4.1. Trace Delays

Table 22: Trace Delays

| Signal Description   | Trace Delay |         |
|--|-------------|---------|
|  | Minimum     | Maximum |
| <b>Adjacent Bus</b> lines: IC1↔IC2<br>(no connections to PSDB)           | 0.5 ns      | 0.6 ns  |
| <b>Adjacent Bus</b> lines: IC2↔IC3, IC 3↔IC4<br>(no connections to PSDB) | 0.4 ns      | 0.5 ns  |
| <b>V18 Bus:</b> IC1↔IC4  | 1.5 ns      | 1.6 ns  |
| <b>V18 Bus:</b> IC1↔IC2  | 0.6 ns      | 0.7 ns  |
| <b>V18 Bus:</b> IC2↔IC3, IC3↔IC4   | 0.5 ns      | 0.6 ns  |
| <b>Main Bus:</b> IC1↔IC2   | 0.55 ns     | 0.6 ns  |
| <b>Main Bus:</b> IC2↔IC3, IC3↔IC4  | 0.45 ns     | 0.5 ns  |
| <b>Main Bus:</b> Total delay   | 1.45 ns     | 1.6 ns  |
| <b>SODIMM Address/Control (All banks)</b>                                | 0.45 ns     | 0.55 ns |
| <b>SODIMM DQ Groups (All banks)</b>                                      | 0.45 ns     | 0.5 ns  |
| <b>Onboard Memory Address/Control</b>                                    | 0.4 ns      | 0.5 ns  |
| <b>Onboard Memory DQ Groups</b>  | 0.15 ns     | 0.20 ns |

\* Performance may change according to the user's implementation (PSDB load and locations).

### 9.4.2. Clock Skews

Table 23: Clock Skews

| Name        | Description   | Maximal Skew |
|-------------|---|--------------|
| $t_{sk1}$   | <p><b>clk0</b> and <b>clk2</b> skew between on-board FPGA devices and the daughterboards (with 1-inch trace on daughterboard)</p> <div style="border: 1px solid black; padding: 2px; width: fit-content; margin: 5px auto;"> <p><b>Note: the 1 inch trace includes 0.4" Board to PSDB distance (PSDB connector length)</b></p> </div> | 50ps         |
| $Osc_{ppm}$ | Oscillator accuracy   | 50ppm        |

### 9.4.3. System I/O Frequency

Table 24: System I/O Frequency

| Path                              | Maximum Frequency |
|-----------------------------------|-------------------|
| Adjacent Bus lines (FPGA to FPGA) | 250 MHz           |
| Main Bus                          | 300 MHz           |
| Link Bus                          | 133 MHz           |
| V18 Bus                           | 300 MHz           |
| L bus to PSDB                     | 250 MHz*          |
| L_IN, R_IN,R_IO,L_IO              | 300 MHz*          |
| Memory bank A (on-board memory)   | 667 MHz (DDR)     |
| Memory bank B (SODIMM)            | 360** MHz (DDR)   |
| Memory bank C (SODIMM)            | 360** MHz (DDR)   |

\* Based on simulation only and is PSDB design dependent

\*\* Only on A speed grade FPGA devices



## 10. Installation

### 10.1. Requirements

The following requirements must be followed in order to compile HDL designs for *PROCStar III* boards:

- An updated Quartus version must be installed on the user's computer in order to compile the HDL designs.
- Ensure that the Quartus computer is at least a Pentium 4 with sufficient memory, normally 1GB, and that the installed Quartus version supports Stratix III devices and their specific packages.

**Note:**

*GiDEL PROC Developer's Kit* and ALTERA Quartus software may run on the same or different computers.

### 10.2. Installing the PROCStar III board

To install the *PROCStar III* perform the following steps:

1. Install *GiDEL PROCDeveloper's Kit* software on the target computer.
2. Turn off the computer.
3. Mount the *PROCStar III* board into the 8 lane PCI Express slot.
4. Secure the board with a screw to the computer's rear panel.
5. Turn on the computer
6. Check that the power LED is on.
7. Allow the Windows operating system to automatically install the *PROCStar III* driver.

**IMPORTANT**

Except for motherboards that support power management, mounting/dismounting the *PROCStar III* board to/from the PCI Express slot when power is ON is **PROHIBITED**. Performing these operations might damage the *PROCStar III* board devices or the PC motherboard.

Mounting/dismounting daughterboards onto/from *PROCStar III* when power is ON is **PROHIBITED**. Performing these operations might damage *PROCStar III* board devices or the daughterboard.

### 10.3. Loading Designs in PCI Express Mode

The Stratix III FPGA is configured (.rbf file loading) via the PCI Express bus by one following options:

- ✓ GiDEL PROCWizard (GiDEL's development software) can automatically load the device(s) at startup. In addition, PROCWizard provides a command that reloads the FPGA in real-time.
- ✓ The user software can load the FPGA through the Application Driver automatically generated by the **PROCWizard**. The design is automatically loaded upon creation of the Application Driver class object or later on by using the **InitIC()** function.

For further information, please refer to the **PROCWizard User's Manual**



## 11. GiDEL Accessories

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### 11.1. GiDEL PROC Developer's Kit™

*GiDEL PROC Developer's Kit* for ASIC/SoC/IP & System Development is a set of building blocks designed for fast, high-productivity system development. It is a complete system solution including boards, software tools, IPs and optional daughterboards. The major software tools and IPs are detailed in the following paragraphs.

### 11.2. GiDEL PROCWizard™

*GiDEL PROCWizard* is an innovative tool that provides a convenient developer environment which automatically generates the hardware/software interface for project level user applications. It has been developed for high system performance. The *PROCWizard* automatically connects between the SW and the HDL applications running on the *PROCSTAR III* system. It generates an application driver (a C++ class) for each application/configuration.

The application driver can be generated for Windows environment. The driver is built in two layers: a Lower Layer and an Upper Layer.

The Lower Layer, the Proc class supplied with the *PROCWizard*, implements basic board functionality such as: FPGA loading, DMA interfaces, interrupt service routines, board clocking system setups, board information acquisition as well as number of FPGAs, their size, speed grade, etc.

The Upper Layer is automatically generated by *PROCWizard*. This class inherits from the Proc class and implements all the application-specific functionality. It loads the Stratix III devices, sets up the board clocking and initializes all the class members to allow simple access to the board application from the user workspace.

The **PROCWizard** can also automatically generate the following:

- HDL code interface module/entity (Verilog, VHDL or AHDL) that communicates with the software driver
- PROCMultiPort (on-board memory controller) instantiations
- Basic PLLs to control external memories
- Top-level design that connects all instantiations with user modules/entities and the on-board local bus and memories
- Device constraints including FPGA pinout, pin power voltage (VCCIO), Quartus operation recommendations, etc.

The **PROCWizard** also enables the user to:

- Test and debug the design in a PC environment
- Access the board with a structural browser and macros/scripts
- Load/save and compare memory files to check data transfers
- Real-time access to the registers/memories defined in the design.
- Documentation generation in HTML or DOC format that describes in detail the generated features

For more information, please refer to the **PROCWizard User's Manual**.

### 11.3. GiDEL PROCMultiPort™

**PROCMultiPort** is a GiDEL IP that provides an advanced controller for on-board memories. This controller has up to 16 ports; each port featuring a simple FIFO or random access.

All ports are connected to the same memory domain and can be accessed independently or simultaneously, with individual clock domains and data widths. **PROCMultiPort** segmented mode provides the ability to logically enlarge the FPGA memory size.

The innovative **PROCMultiPort** concept enables new design methodologies that can replace many large and complicated designs, thus reducing the development effort. For example, it can replace swappable double buffers or implement multiple logical memories in the same physical memory.

For more information, please refer to the **PROCMultiPort IP User's Guide**.

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## 11.4. GiDEL **PROC***MegaDelay*<sup>TM</sup>

**PROC***MegaDelay* is a GiDEL IP that provides a simple and convenient way to create large delay lines/frame delays. **PROC***MegaDelay* eliminates the need to use standard delay lines utilizing internal FPGA memories. Instead, it uses the on-board memory, thus enabling generation of very large delay lines.

**PROC***MegaDelay* is typically used for 2D/3D video processing, where very large quantities of data must be stored in memory and extracted later. **PROC***MegaDelay* makes it possible to compare two (not necessary consecutive) video frames, or to write video stream as it arrives, and read it frame by frame for further processing.

For more information, please refer to the **PROC***MegaDelay* IP User's Guide.

## 11.5. GiDEL **PROC***MegaFIFO*<sup>TM</sup>

**PROC***MegaFIFO* is a GiDEL IP that provides a simple and convenient way to transfer data to/from GiDEL **PROC** boards. With **PROC***MegaFIFO*, using the on-board memory as a very large FIFO, data may be transferred between the host PC and user's sub-designs, or between sub-designs.

**PROC***MegaFIFO* eliminates the need to take care of synchronization when transferring data between designs. The software no longer needs to respond to the hardware in real-time. Hardware designs may now transfer data in bursts and withdraw it in a continuous stream.

**PROC***MegaFIFO* uses special arbitration techniques when transferring data between the host PC and user's sub-designs. These techniques prevent memory overflows/underuse, thus using the maximum available bandwidth for data transfers.

Request and Acknowledge signals ensure correct data transfers. On the software side, the Proc class methods perform automatic initialization of the FIFO logic and enable easy data transfers by using DMA.

For more information, please refer to the **PROC***MegaFIFO* IP User's Guide.

## 11.6. **PSDB**\_Proto<sup>TM</sup>

**PSDB**\_Proto is a **PROC**Star III daughterboard (PSDB2) for rapid system connection. It enables to wire-warp or to solder external devices and connectors to the board. It also can function as a logic analyzer adapter. The PSDB I/Os are directly connected to the Mictor and the Soft\_Touch connectors.



### 12.1. Throughput Calculations

#### 12.1.1. M9K Throughput Calculations

Largest bit width configuration of the M9K block : **18 bit**

Width in true dual-port mode: 2x36 bit = 72 bit = **9 Byte**

Maximum M9K blocks usage in four 340L devices: **4160**

Typical performance: **300 MHz**

**M9K throughput = 9 x 4160 x 300 ≈ 11,000 GB/s**

#### 12.1.2. M144K Throughput Calculations

Largest bit width configuration of the M9K block: **36 bit**

Width in true dual-port mode: 2x72 bit = 144 bit = **18 Byte**

Maximum M9K blocks in four 260E devices: **192**

Typical performance: **300 MHz**

**M144K throughput = 18 x 192 x 300 ≈ 1,000 GB/s**

#### 12.1.3. On-board Memories Throughput Calculations

The onboard memory performs at 667 MHz (DDR) using a 8-byte wide bus. The PROCMultiPort controller enables 75% DRAM access-rate efficiency. There are 4 on-board memory modules on 4 FPGA device board.

Thus, **throughput = 667MHz×8×0.75×4 ≈ 16 GB/s**

#### 12.1.4. SODIMM Throughput Calculations

The SODIMM performs at 360 MHz (DDR) via an 8-byte wide bus. The PROCMultiPort controller enables 75% DRAM access-rate efficiency. There are up to 8 SODIMM modules on a 4 FPGA device board.

Thus, **throughput = 360 MHz×8×0.75×8 = 1900 MB/s ≈ 17 GB/s.**

## 12.2. Additional Devices Needed

- ✓ Fuse: FB 7A-MQ PIC BEL.
- ✓ Connector sockets for user PSDB: QTH-060-XX-F-D-A (Samtec), where XX specifies the connector height as shown in Table 25:

Table 25: PSDB Connector Heights.

| XX   | Height        |
|------|---------------|
| - 01 | (5,00) .198   |
| - 02 | (8,00) .316   |
| - 03 | (11,00) .434  |
| - 09 | (14,00) .552  |
| - 04 | (16,00) .630  |
| - 05 | (19,00) .748  |
| - 06 | (22,00) .866  |
| - 07 | (25,00) .984  |
| - 08 | (30,00) 1,181 |

- ✓ DDR II SODIMM modules. For listing of *PROCStar III* compatible DDR II SODIMM modules, refer to the *SODIMM Type DataSheet* document.



## 13. References

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### 13.1. References

- *Stratix III Device Handbook, Altera Corporation*
- *PROCWizard Version 8.0 User's Manual*
- *PROCMultiPort IP User Guide*
- *PROC Internal Bus Data Book*
- *PSDB1 Reference Guide*
- *PSDB2 Reference Guide*
- *PSDB\_Mem II Data Book*



## 14. Glossary

Table 26: Table of Acronyms

| ACRONYMS | DESCRIPTION                             |
|----------|---|
| ASIC     | Application Specific Integrated Circuit |
| DDR      | Double Data Rate                        |
| DRAM     | Dynamic Random Access Memory            |
| FPGA     | Field Programmable Gate Array           |
| IP       | Intellectual Property                   |
| LVDS     | Low Voltage Differential Signaling      |
| MTBF     | Mean Time Between Failures              |
| PCB      | Printed Circuit Board                   |
| PLL      | Phased-Locked Loop                      |
| PSDB     | PROCStar III Daughterboard              |
| RTL      | Register Transfer Logic                 |
| SoC      | System-on-Chip                          |
| IC       | Integrated Circuit                      |



## 15. Revision History

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### 15.1. PCB History

| Revision | Changes  |
|----------|--|
| Rev 1    | Initial board                                  |
| Rev 2    | Resolved potential configuration problems      |
| Rev 3    | Resolved support problems for 340 FPGA devices |

### 15.2. POF – Board Controller History

| Revision | Changes                          |
|----------|----------------------------------|
| 30       | Initial code                     |
| 31       | Support for PSDB_DSP             |
| 32       | Support for Rev2 and Rev3 boards |

## 15.3. PROCStar III Data Book History

| Date    | Changes   |
|---------|---|
| 01/2008 | Data Book Version 1.0   |
| 03/2008 | <ul style="list-style-type: none"> <li>• Addition of DDRII SDRAM pin-out and signal connectivity</li> <li>• Explanation on DMA setting via PROCWizard</li> </ul>  |
| 04/2008 | <ul style="list-style-type: none"> <li>• Update of suitable DDRII modules</li> </ul>  |
| 06/2008 | Update of the following: <ul style="list-style-type: none"> <li>• Ch. 3: addition of more models</li> <li>• Sec. 6.2 PSB Placements</li> <li>• Sec. 9.2 Electrical and Mechanical Environment</li> <li>• Sec. 9.4 Power Consumption</li> <li>• Sec. 9.5 Timing Model</li> </ul> |
| 08/2008 | Update of the following: <ul style="list-style-type: none"> <li>• Ch.3: Standard Models</li> <li>• Table 19: Trace Delays</li> </ul>  |
| 12/08   | Update of Memory Throughput calculations  |
| 01/08   | Added 7.4.2 DDRII DRAM SODIMM connectivity and pinout diagram<br>Deleted all references to Ethernet and Stand-alone mode.<br>Updated Memory Throughput calculations   |