

Official CHREC Publications (IAB supported & approved)

2011

Project	Publication	File
F1	V. Aggarwal, G. Stitt, A. George and C. Yoon, "SCF: A Framework for Task-Level Coordination in Reconfigurable, Heterogeneous Systems," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , to appear.	TBA
B6	N. Rollins and M. Wirthlin, "Software Fault-Tolerant Techniques for Softcore Processors in Commercial SRAM-Based FPGAs," <i>Microprocessors and Microsystems</i> journal, to appear.	TBA
B5	B. Pratt, M. Fuller, and M. Wirthlin, "Reduced-Precision Redundancy on FPGAs," <i>International Journal on Reconfigurable Computing</i> , to appear.	TBA
G6	M. Huang, V. K. Narayana, M. Bakhouya, J. Gaber and T. El-Ghazawi, "Efficient Mapping of Task Graphs onto Reconfigurable Hardware Using Architectural Variants," <i>IEEE Transactions on Computers (TC)</i> , to appear.	TBA
F1	S. Koehler, G. Stitt, and A. George, "Platform-Aware Bottleneck Detection for Reconfigurable Computing Applications," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , to appear.	TBA
F5	N. Wulf, A. George, and A. Gordon-Ross, "A Framework to Analyze, Compare, and Optimize High-Performance, On-Board Processing Systems," <i>Proc. of IEEE Aerospace Conference</i> , Big Sky, MT, Mar. 3-10, 2012.	TBA
F6	S. Arnold, R. Nuzzaci, J. Antoon, and A. Gordon-Ross, "Energy Budgeting for CubeSats with an Integrated FPGA," <i>Proc. of IEEE Aerospace Conference</i> , Big Sky, MT, Mar. 3-10, 2012.	TBA
F3	R. Kirchgessner, G. Stitt, A. George, and H. Lam, "VirtualRC: A Virtual FPGA Platform for Applications and Tools Portability," <i>Proc. of International ACM/SIGDA Symposium on Field Programmable Gate Arrays (FPGA)</i> , Monterey, CA, Feb. 22-24, 2012.	TBA
F1	J. Curreri, G. Stitt, and A. George, "Communication Visualization for Bottleneck Detection of High-Level Synthesis Applications," <i>Proc. of International ACM/SIGDA Symposium on Field Programmable Gate Arrays (FPGA)</i> , Monterey, CA, Feb. 22-24, 2012.	TBA
F4	A. Jara-Berrocal and A. Gordon-Ross, "Hardware Module Reuse and Runtime Assembly for Dynamic Management of Reconfigurable Resources," <i>Proc. of IEEE International Conference on Field-Programmable Technology (FPT)</i> , Dec. 12-14, 2011.	TBA
F4	S. Yousuf and A. Gordon-Ross, "Partially Reconfigurable System-on-Chips for Adaptive Fault Tolerance," <i>Proc. of IEEE International Conference on Field-Programmable Technology (FPT)</i> , Dec. 12-14, 2011.	TBA
F4	R. Kumar and A. Gordon-Ross, "Formulation-level Design Space Exploration for Partially Reconfigurable FPGAs," <i>Proc. of IEEE International Conference on Field-Programmable Technology (FPT)</i> , Dec. 12-14, 2011.	TBA
G9	T. Li, V. K. Narayana and T. El-Ghazawi, "A Static Task Scheduling Framework for Independent Tasks Accelerated using a Shared Graphics Processing Unit," <i>Proc. of 17th International Conference on Parallel and Distributed Systems (ICPADS)</i> , Tainan, Taiwan, Dec. 7-9, 2011.	TBA

G8	A. Anbar, O. Serres and T. El-Ghazawi, "Reflex Barrier: A Scalable Network-Based Synchronization Barrier," <i>Proc. of 17th International Conference on Parallel and Distributed Systems (ICPADS)</i> , Tainan, Taiwan, Dec. 7-9, 2011.	TBA
V1	M.Elteir, H. Lin, W. Feng, and T. Scogland, "StreamMR: An Optimized MapReduce Framework for AMD GPUs," <i>Proc. of IEEE International Conference on Parallel and Distributed Systems (ICSPADS)</i> , Tainan, Taiwan, Dec. 7-9, 2011.	TBA
V1	M. Elteir, T. Scogland, and W. Feng, "Architecture-Aware Mapping and Optimization on a 1600-Core GPU," <i>Proc. of IEEE International Conference on Parallel and Distributed Systems (ICSPADS)</i> , Tainan, Taiwan, Dec. 7-9, 2011.	TBA
V1	K. Pereira, P. Athanas, H. Lin, and W. Feng, "Spectral Method Characterization of FPGA and GPU Accelerators," <i>Proc. of International Conference on Reconfigurable Computing and FPGAs (ReConFig)</i> , Cancun, Mexico, Nov. 30 - Dec. 2, 2011.	TBA
G8	O. Serres, V.K. Narayana and T. El-Ghazawi, "An Architecture for Reconfigurable Multi-core Explorations," <i>Proc. of International Conference on Reconfigurable Computing and FPGAs (ReConFig)</i> , Cancun, Mexico, Nov. 30 - Dec. 2, 2011.	TBA
F1	G. Stitt and J. Coole, "Intermediate Fabrics: Virtual Architectures for Near-Instant FPGA Compilation," <i>IEEE Embedded Systems Letters</i> , Special Issue on Embedded Reconfigurable Computing Systems, Vol. 3, No. 3, Sep. 2011, pp. 81-84.	TBA
V1	M. Elteir, H. Lin, and W. Feng, "Performance Characterization and Optimization of Atomic Operations on AMD GPUs," <i>Proc. of IEEE Cluster conference</i> , Austin, TX, Sep. 26-30, 2011.	TBA
F4	A. Jara-Berrocal and A. Gordon-Ross, "An Integrated Development Toolset and Implementation Methodology for Partially Reconfigurable System-on-Chips," <i>IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)</i> , Santa Monica, CA, Sep. 11-14, 2011.	PDF
B1	C. Lavin, M. Padilla, J. Lamprecht, P. Lundrigan, B. Nelson and B. Hutchings, "RapidSmith: Do-It-Yourself CAD Tools for Xilinx FPGAs," <i>Proc. of International Conference on Field-Programmable Logic and Applications (FPL)</i> , Chania, Crete, Sep. 5-7, 2011.	TBA
B1	S. Ghosh and B. Nelson, "XDL-Based Module Generators for Rapid FPGA Design Implementation," <i>Proc. of International Conference on Field-Programmable Logic and Applications (FPL)</i> , Chania, Crete, Sep. 5-7, 2011.	TBA
F1	G. Stitt, A. George, H. Lam, M. Smith, V. Aggarwal, G. Wang, C. Reardon, B. Holland, S. Koehler, and J. Coole, "An End-to-End Tool Flow for FPGA-Accelerated Scientific Computing," <i>IEEE Design & Test of Computers (D&T)</i> , Vol. 28, No. 4, July/Aug. 2011, pp. 68-77.	TBA
V1	M. Daga, A. Aji, and W. Feng, "On the Efficacy of a Fused CPU+GPU Processor for Parallel Computing," <i>Proc. of Symposium on Application Accelerators in High-Performance Computing (SAAHPC)</i> , Knoxville, TN, July 19-20, 2011.	TBA
G8	O. Serres, A. Anbar, S. G. Merchant, A. Kayi and T. El-Ghazawi, "Address translation optimization for Unified Parallel C multi-dimensional arrays," <i>Proc. of 16th International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS)</i> at IPDPS'11, Anchorage, AK, May 20, 2011.	PDF
B1	C. Lavin, M. Padilla, J. Lamprecht, P. Lundrigan, B. Nelson, and B. Hutchings, "HMFlow: Accelerating FPGA Compilation with Hard Macros for Rapid Prototyping," <i>Proc. of 18th IEEE Symposium on Field-Programmable</i>	PDF

	<i>Custom Computing Machines (FCCM)</i> , Salt Lake City, UT, May 1-3, 2011.	
F6	N. Wulf, G. Cieslewski, A. Gordon-Ross, and A. George, "SCIPS: An Emulation Methodology for Fault Injection in Processor Caches," <i>Proc. of IEEE Aerospace Conference (AERO)</i> , Big Sky, MT, Mar. 5-12, 2011.	PDF
B6	K. Ellsworth, T. Haroldsen, B. Nelson, and M. Wirthlin, "Dual Channel Architecture for Reliable FPGA high Speed Serial Links," <i>Proc. of IEEE Aerospace Conference (AERO)</i> , Big Sky, MT, Mar. 5-12, 2011.	PDF
G8	O. Serres, A. Anbar, S. Merchant and T. El-Ghazawi, "Experiences with UPC on TILE-64 processor," <i>Proc. of IEEE Aerospace Conference (AERO)</i> , Big Sky, MT, Mar. 5-12, 2011.	PDF
B6	N. Rollins and M. Wirthlin, "Software Fault-Tolerant Techniques for Softcore Processors in Commercial SRAM-Based FPGAs," <i>Proc. of 1st Workshop on Software-Controlled, Adaptive Fault-Tolerance in Microprocessors (SCAFT)</i> , Como, Italy, Feb. 22, 2011.	PDF
F3	A. George, H. Lam, and G. Stitt, "Novo-G: At the Forefront of Scalable Reconfigurable Computing," <i>IEEE Computing in Science & Engineering (CiSE)</i> , Vol. 13, No. 1, Jan/Feb. 2011, pp. 82-86.	PDF
F1	J. Curreri, G. Stitt, and A. George, "High-level Synthesis of In-Circuit Assertions for Verification, Debugging, and Timing Analysis," <i>International Journal of Reconfigurable Computing (IJRC)</i> , special issue of extended best papers from IPDPS/RAW'10, Vol. 2011, Article No. 406857, Jan. 2011, 17 pages.	PDF

2010

Project	Publication	File
B6	Y. Li, B. Nelson, and M. Wirthlin, "Synchronization Techniques for Crossing Multiple Clock Domains in FPGA-Based TMR Circuits," <i>IEEE Transactions On Nuclear Science (TNS)</i> , Vol. 57, No. 6, Dec. 2010, pp. 3506-3514.	PDF
B1	C. Lavin, M. Padilla, J. Lamprecht, P. Lundrigan, B. Nelson, and B. Hutchings, "Rapid Prototyping Tools for FPGA Designs: RapidSmith," <i>Proc. of International Conference on Field-Programmable Technology (FPT)</i> , Beijing, China, Dec. 8-10, 2010.	PDF
F1	S. Craciun, A. George, H. Lam, and J. Principe, "A Parallel Hardware Architecture for Information-Theoretic Adaptive Filtering," <i>Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA)</i> at SC'10, New Orleans, LA, Nov. 14, 2010.	PDF
F5	J. Richardson, S. Fingulin, D. Raghunathan, C. Massie, A. George, and H. Lam, "Comparative Analysis of HPC and Accelerator Devices: Computation, Memory, I/O, and Power," <i>Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA)</i> at SC'10, New Orleans, LA, Nov. 14, 2010.	PDF
F5	J. Williams, A. George, J. Richardson, K. Gosrani, C. Massie, and H. Lam, "Characterization of Fixed and Reconfigurable Multi-Core Devices for Application Acceleration," <i>ACM Transactions on Reconfigurable Technology and Systems (TRETS)</i> , Vol. 3, No. 4, Nov. 2010, pp. 19:1-19:29.	PDF
G6	M. Huang, V. K. Narayana, H. Simmler, O. Serres, and T. El-Ghazawi, "Reconfiguration and Communication-Aware Task Scheduling for High-Performance Reconfigurable Computing," <i>ACM Transactions on Reconfigurable Technology and Systems (TRETS)</i> , Vol. 3, No. 4, Nov. 2010, pp. 20:1-20:25.	PDF

F1	C. Reardon, E. Grobelny, A. George, and G. Wang, "A Simulation Framework for Rapid Analysis of Reconfigurable Computing Systems," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , Vol. 3, No. 4, Nov. 2010, pp. 25:1-25:29.	PDF
F1	B. Holland, A. George, H. Lam, and M. Smith, "An Analytical Model for Multi-Level Performance Prediction of Multi-FPGA Systems," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , to appear.	TBA
F2	J. Coole and G. Stitt, "Intermediate Fabrics: Virtual Architectures for Circuit Portability and Fast Placement and Routing," <i>Proc. of International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)</i> , Scottsdale, AZ, Oct. 24-29, 2010, to appear.	PDF
B5	M. Rice, B. Nelson, M. Padilla, and J. Havican, "On The Use of Rapid Prototyping for Designing PCM/FM Demodulators in FPGAs," <i>Proc. of 2010 International Telemetering Conference (ITC)</i> , Las Vegas NV, Oct. 24-27, 2010.	PDF
F1	V. Aggarwal, C. Yoon, A. George, H. Lam, and G. Stitt, "Performance Modeling for Multilevel Communication in SHMEM+," <i>Proc. of Conference on Partitioned Global Address Space Programming Model (PGAS)</i> , New York, NY, Oct. 12-15, 2010, to appear.	PDF
F1	V. Aggarwal, A. George, C. Yoon, K. Yalamanchili, and H. Lam, "SHMEM+: A Multilevel-PGAS Programming Model for Reconfigurable Supercomputing," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , to appear.	PDF
V1	T. Scogland, H. Lin, and W. Feng, "A First Look at Integrated GPUs for Green High-Performance Computing," <i>Proc. of International Conference on Energy-Aware High-Performance Computing (EnA-HPC)</i> , Stuttgart, Germany, Sep. 16-17, 2010.	TBA
B1	A. Arnesen, K. Ellsworth, D. Gibelyou, T. Haroldsen, J. Havican, M. Padilla, B. Nelson, M. Rice, and M. Wirthlin, "Increasing Design Productivity Through Core Reuse, Meta-Data Encapsulation, and Synthesis," <i>Proc. of International Conference on Field-Programmable Logic and Applications (FPL)</i> , Aug. 31 - Sep. 2, 2010.	PDF
B1	C. Lavin, M. Padilla, S. Ghosh, B. Nelson, B. Hutchings, and M. Wirthlin, "Using Hard Macros to Reduce FPGA Compilation Time," <i>Proc. of International Conference on Field-Programmable Logic and Applications (FPL)</i> , Aug. 31 - Sep. 2, 2010.	PDF
F1	C. Pascoe, A. Lawande, H. Lam, A. George, Y. Sun, W. Farmerie, and M. Herbordt, "Reconfigurable Supercomputing with Scalable Systolic Arrays and In-Stream Control for Wavefront Genomics Processing," <i>Proc. of Symposium on Application Accelerators in High-Performance Computing (SAAHPC)</i> , Knoxville, TN, July 13-15, 2010.	PDF
F1	C. Reardon, A. George, G. Stitt, and H. Lam, "An Automated Scheduling and Partitioning Algorithm for Scalable RC Systems," <i>Proc. of International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)</i> , Las Vegas, NV, July 12-15, 2010.	PDF
F6	G. Cieslewski, A. George, and A. Jacobs, "Acceleration of FPGA Fault Injection through Multi-Bit Testing," <i>Proc. of International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)</i> , Las Vegas, NV, July 12-15, 2010.	PDF
F1	B. Holland, A. George, and H. Lam, "Integrating Application Specification and Performance Prediction for Strategic Design-Space Exploration," <i>Proc. of International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)</i> , Las Vegas, NV, July 12-15, 2010.	PDF

F4	S. Yousuf and A. Gordon-Ross, "DAPR: Design Automation for Partially Reconfigurable FPGAs," <i>Proc. of International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)</i> , Las Vegas, NV, July 12-15, 2010.	PDF
F2	S. Koehler and A. George, "Performance Visualization and Exploration for Reconfigurable Computing Applications," <i>Proc. of International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)</i> , Las Vegas, NV, July 12-15, 2010.	PDF
V1	R. Anandakrishnan, T. Scogland, A. Fenley, J. Gordon, W. Feng, and A. Onufriev, "Accelerating Electrostatic Surface Potential Calculation with Multiscale Approximation on Graphics Processing Units," <i>Journal of Molecular Graphics Modelling (JMGM)</i> , Vol. 28, No. 8, June 2010, pp. 904-910.	PDF
B5a	B. Pratt, M. Fuller, M. Rice, and M. Wirthlin, "Reliable Communications Using FPGAs in High-Radiation Environments - Part I: Characterization," <i>Proc. of IEEE International Conference on Communications (ICC)</i> , Cape Town, South Africa, May 23-27, 2010.	PDF
B2	J. Bodily, B. Nelson, Z. Wei, D. Lee, and J. Chase, "A Comparison Study on Implementing Optical Flow and Digital Communications on FPGAs and GPUs," <i>ACM Transactions on Reconfigurable Technology and Systems (TRETS)</i> , Vol. 3, No. 2, May 2010, pp. 1-22.	PDF
G4	E. El-Araby, S. Merchant, and T. El-Ghazawi, "A Framework for Evaluating High-Level Design Methodologies for High-Performance Reconfigurable Computers," <i>IEEE Transactions on Parallel and Distributed Systems (TPDS)</i> , preprint version available on-line.	PDF
F2	J. Curreri, G. Stitt, and A. George, "High-Level Synthesis Techniques for In-Circuit Assertion-Based Verification," <i>Proc. of 17th Reconfigurable Architectures Workshop (RAW)</i> at IPDPS'10, Atlanta, GA, Apr. 19-20, 2010.	PDF
F1	C. Reardon, B. Holland, A. George, G. Stitt, and H. Lam, "RCML: An Environment for Estimation Modeling of Reconfigurable Computing Systems," <i>ACM Transactions on Embedded Computing Systems (TECS)</i> , to appear.	PDF
G7	E. El-Araby, V. Narayana, and T. El-Ghazawi, "Space and Time Sharing of Reconfigurable Hardware for Accelerated Parallel Processing," <i>Proc. of 6th International Symposium on Applied Reconfigurable Computing (ARC)</i> , Bangkok, Thailand, March 17-19, 2010.	PDF
F4	A. Jara-Berrocal and A. Gordon-Ross, "VAPRES: A Virtual Architecture for Partially Reconfigurable Embedded Systems," <i>Proc. of Design, Automation, and Test in Europe (DATE) Conference</i> , Grenoble, France, Mar. 14-18, 2010.	PDF
B5b	N. Rollins, M. Fuller, and M. Wirthlin, "A Comparison of Fault-Tolerant Memories in SRAM-Based FPGAs," <i>Proc. of IEEE Aerospace Conference (AERO)</i> , Big Sky, MT, Mar. 6-13, 2010.	PDF
B5a	J. Anderson, B. Nelson, and M. Wirthlin, "Using Statistical Models with Duplication and Compare for Reduced Cost FPGA Reliability," <i>Proc. of IEEE Aerospace Conference (AERO)</i> , Big Sky, MT, Mar. 6-13, 2010.	PDF
B3	J. Johnson and M. Wirthlin, "Voter Insertion Algorithms for FPGA Designs Using Triple Modular Redundancy," <i>Proc. of ACM SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)</i> , Monterey, CA, Feb. 21-23, 2010.	PDF
F2	J. Curreri, S. Koehler, A. George, B. Holland, and R. Garcia, "Performance Analysis Framework for High-Level Language Applications in Reconfigurable Computing," <i>ACM Transactions on Reconfigurable Technology and Systems (TRETS)</i> , Vol. 3, No. 1, Jan. 2010, pp. 1-23.	PDF

Project	Publication	File
B3	P. Ostler, M. Caffrey, D. Gibelyou, P. Graham, K. Morgan, B. Pratt, H. Quinn, and M. Wirthlin, "SRAM FPGA Reliability Analysis for Harsh Radiation Environments," <i>IEEE Transactions on Nuclear Science (TNS)</i> , Vol. 56, No. 6, Dec. 2009, pp. 3519-3526.	PDF
F4	A. Jara-Berrocal and A. Gordon-Ross, "Runtime Temporal Partitioning Assembly to Reduce FPGA Reconfiguration Time," <i>Proc. of International Conference on Reconfigurable Computing and FPGAs (ReConFig)</i> , Cancun, Mexico, Dec. 9-11, 2009.	PDF
F1	V. Aggarwal, A. George, K. Yalamanchili, C. Yoon, H. Lam, and G. Stitt, "Bridging Parallel and Reconfigurable Computing with Multilevel PGAS and SHMEM+," <i>Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA)</i> at SC'09, Portland, OR, Nov. 15, 2009. Winner of the OpenFPGA paper award.	PDF
F1	V. Aggarwal, R. Garcia, G. Stitt, A. George, and H. Lam, "SCF: A Device- and Language-Independent Task Coordination Framework for Reconfigurable, Heterogeneous Systems," <i>Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA)</i> at SC'09, Portland, OR, Nov. 15, 2009.	PDF
F1	G. Wang, G. Stitt, H. Lam, and A. George, "A Framework for Core-level Modeling and Design of Reconfigurable Computing Algorithms," <i>Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA)</i> at SC'09, Portland, OR, Nov. 15, 2009.	PDF
F4	S. Yousuf and A. Gordon-Ross, "Run-Time FPGA Partial Reconfiguration for Image Processing Applications," <i>Proc. of Military and Aerospace Programmable Logic Devices Conference (MAPLD)</i> , Greenbelt, MD, Aug. 31 - Sep. 3, 2009.	PDF
B5b	N. Rollins and M. Wirthlin, "Fault-Tolerant Block-RAM Memories in SRAM-Based FPGAs," <i>Proc. of Military and Aerospace Programmable Logic Devices Conference (MAPLD)</i> , Greenbelt, MD, Aug. 31 - Sep. 3, 2009.	PDF
B5a	J. Anderson, B. Nelson, and M. Wirthlin, "Reduced Cost Reliability via Statistical Model Detection," <i>Proc. of Military and Aerospace Programmable Logic Devices Conference (MAPLD)</i> , Greenbelt, MD, Aug. 31 - Sep. 3, 2009.	PDF
B5b	Y. Li, B. Nelson, and M. Wirthlin, "Synchronization Issues of TMR Crossing Multiple Clock Domains," <i>Proc. of Military and Aerospace Programmable Logic Devices Conference (MAPLD)</i> , Greenbelt, MD, Aug. 31 - Sep. 3, 2009.	PDF
F6	G. Cieslewski and A. George, "SPFFI: Simple Portable FPGA Fault Injector," <i>Proc. of Military and Aerospace Programmable Logic Devices Conference (MAPLD)</i> , Greenbelt, MD, Aug. 31 - Sep. 3, 2009.	PDF
B1	M. Rice, M. Padilla, and B. Nelson, "On FM Demodulators in Software-Defined Radios Using FPGAs," <i>Proc. of Military Communications Conference (MILCOM)</i> , Boston, MA, Oct. 18-21, 2009.	PDF
B2	B. Hutchings, B. Nelson, S. West, and R. Curtis, "Comparing Fine-Grained Performance on the Ambric MPPA Against an FPGA," <i>Proc. of Intl. Conference on Field-Programmable Logic and Applications (FPL)</i> , Prague, Czech Republic, Aug. 31 - Sep. 2, 2009.	PDF

F6	A. Jacobs, A. George, and G. Cieslewski, "Reconfigurable Fault Tolerance: A Framework for Environmentally Adaptive Fault Mitigation in Space," <i>Proc. of Intl. Conference on Field-Programmable Logic and Applications (FPL)</i> , Prague, Czech Republic, Aug. 31 - Sep. 2, 2009.	PDF
B1	A. Arnesen, N. Rollins, and M. Wirthlin, "A Multi-Layered XML Schema and Design Tool for Reusing and Integrating FPGA IP," <i>Proc. of Intl. Conference on Field-Programmable Logic and Applications (FPL)</i> , Prague, Czech Republic, Aug. 31 - Sep. 2, 2009.	PDF
B3	B. Pratt, M. Wirthlin, M. Caffrey, P. Graham, and K. Morgan, "Noise Impact of Single-Event Upsets on an FPGA-Based Digital Filter," <i>Proc. of Intl. Conference on Field-Programmable Logic and Applications (FPL)</i> , Prague, Czech Republic, Aug. 31 - Sep. 2, 2009.	PDF
F4	R. Kumar and A. Gordon-Ross, "MACS: A Minimal Adaptive Routing Circuit-Switched Architecture for Scalable and Parametric NoCs," <i>Proc. of Intl. Conference on Field-Programmable Logic and Applications (FPL)</i> , Prague, Czech Republic, Aug. 31 - Sep. 2, 2009.	PDF
F5	J. Richardson, C. Massie, H. Lam, K. Gosrani, and A. George, "Space Applications on Tiler," Workshop for Multicore Processors For Space - Opportunities and Challenges, <i>IEEE International Conference on Space Mission Challenges for Information Technology (SMC-IT)</i> , Pasadena, CA, July 19-23, 2009.	PDF
F6	A. Jacobs, G. Cieslewski, and A. George, "Adaptive Software-based Fault Tolerance for Space Multicore Processing," Workshop for Multicore Processors For Space - Opportunities and Challenges, <i>IEEE International Conference on Space Mission Challenges for Information Technology (SMC-IT)</i> , Pasadena, CA, July 19-23, 2009.	PDF
F1/F3	K. Nagarajan, B. Holland, A. George, K. Slatton, and H. Lam, "Accelerating Machine-Learning Algorithms on FPGAs using Pattern-Based Decomposition," <i>Journal of Signal Processing Systems (JSPS)</i> , preprint version available on-line.	PDF
G7	E. El-Araby, I. Gonzalez, and T. El-Ghazawi, "Exploiting Partial Run-Time Reconfiguration for High-Performance Reconfigurable Computing," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , Vol. 1, No. 4, Jan. 2009, pp. 21:1-21:23.	PDF
F1/F3	B. Holland, K. Nagarajan, and A. George, "RAT: RC Amenability Test for Rapid Performance Prediction," <i>ACM Transactions on Reconfigurable Technology and Systems (TRET)</i> , Vol. 1, No. 4, Jan. 2009, pp. 22:1-22:31.	PDF
G6	M. Huang, H. Simmler, O. Serres, and T. El-Ghazawi, "RDMS: A Hardware Task Scheduling Algorithm for Reconfigurable Computing," <i>Proc. of 16th Reconfigurable Architectures Workshop (RAW)</i> , Rome, Italy, May 25-26, 2009.	PDF
F4	A. Flynn, A. Gordon-Ross, and A. George, "Bitstream Relocation with Local Clock Domains for Partially Reconfigurable FPGAs," <i>Proc. of Design, Automation, and Test in Europe (DATE) Conference</i> , Nice, France, Apr. 20-24, 2009.	PDF
F4	A. Jara-Berrocal and A. Gordon-Ross, "SCORES: A Scalable and Parametric Streams-Based Communication Architecture for Modular Reconfigurable Systems," <i>Proc. of Design, Automation, and Test in Europe (DATE) Conference</i> , Nice, France, Apr. 20-24, 2009.	PDF
G6	M. Huang, V. Narayana, and T. El-Ghazawi, "Efficient Mapping of Hardware Tasks on Reconfigurable Computers using Libraries of Architecture Variants," <i>Proc. of 16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)</i> , Napa, CA, Apr. 5-7, 2009.	PDF

B3	M. Caffrey, M. Wirthlin, W. Howes, D. Richins, D. Roussel-Dupre, S. Robinson, A. Nelson, and A. Salazar, "On-Orbit Flight Results from the Reconfigurable Cibola Flight Experiment Satellite (CFESat)," <i>Proc. of 16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)</i> , Napa, CA, Apr. 5-7, 2009.	PDF
B2	B. Hutchings, B. Nelson, S. West, and R. Curtis, "Implementing Optical Flow on the Ambric AM2045 MPAA," <i>Proc. of 16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)</i> , Napa, CA, Apr. 5-7, 2009.	PDF
F4	R. Garcia, A. Gordon-Ross, and A. George, "Exploiting Partially Reconfigurable FPGAs for Situation-Based Reconfiguration in Wireless Sensor Networks," <i>Proc. of 16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)</i> , Napa, CA, Apr. 5-7, 2009.	PDF

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G7	E. El-Araby, I. Gonzalez, and T. El-Ghazawi, "Virtualizing and Sharing Reconfigurable Resources in High-Performance Reconfigurable Computing Systems," <i>Proc. of High-Performance Reconfigurable Computing Technology and Applications Workshop (HPRCTA)</i> at SC'08, Austin, TX, Nov. 17, 2008.	PDF
V2	A. Aji and W. Feng, "Optimizing Performance, Cost, and Sensitivity in Pairwise Sequence Search on a Cluster of PlayStations," <i>Proc. of 8th IEEE International Conference on BioInformatics and BioEngineering (BIBE)</i> , Athens, Greece, Oct. 8-10, 2008.	PDF
F5	J. Williams, A. George, J. Richardson, K. Gosrani, and S. Suresh, "Fixed and Reconfigurable Multi-Core Device Characterization for HPEC," <i>Proc. of High-Performance Embedded Computing Workshop (HPEC)</i> , Lexington, MA, Sep. 23-25, 2008.	PDF
F4	G. Cieslewski, C. Conger, A. George, and B. Kilpatrick, "Reconfigurable Fault Tolerance for FPGA-based Space Computing," <i>Proc. of Military and Aerospace Programmable Logic Devices Conference (MAPLD)</i> , Annapolis, MD, September 15-18, 2008.	PDF
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