

EXECUTIVE SUMMARY

PROJECT NAME: V3-09 - Autonomous Adaptive Systems

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PROJECT DESCRIPTION

Many of the projects and applications developed within CHREC have an underlying reliance on vendor tools. While it is likely impractical to break from the vendor tools completely, offering a higher degree of independence can expand the dynamic properties of CHREC applications. The purpose of this task is to ultimately make a system that is to a degree "self-aware" and can configure itself autonomously at a fine granularity in response to external stimuli. A system with these capabilities could do system-level link maintenance (cognitive and software-defined radios), change the topology of a computation (HPC), universal modularity for in-system adaptation, or rework a system in response to a highly localized failure.

EXPERIMENTAL PLAN

Task 1: Create connectivity database for contemporary FPGAs. For a system to function autonomously, it must be able to account for its own logic. The autonomous system must be able to manipulate a logical structure (database) modeling it's own functionality.

Task 2: Form compact connectivity model that can be embedded. APIs and support utilities are needed for the embedded Linux

Task 3: Form compact logic model for mapping changes. As with the connectivity model, an internal logic model must be created. An autonomous system must be able to express an incremental change (EDIF) into available FPGA resources.

Risk exists in that many of the core capabilities don't yet exist for the Virtex-5 devices. As a backup, work will shift to Virtex-4 devices.

HOW THIS PROJECT IS DIFFERENT

Unlike other approaches that work at a module or regional granularity, this task focuses on the manipulation of individual wires and gates, giving a system the "knowledge" of what resources are in use and can be altered.

POTENTIAL MEMBER COMPANY BENEFITS

This provides a new use-model for FPGAs that could create new capabilities to members' products, and provide a potentially new method for fault recovery. This extends the concept of *RCML*, created in F1-08, from being a design-creation language to a run-time operational language. In a similar fashion, the concepts of B1-08 are enhanced in the way to offer more flexibility in core library instantiation within designs.

EXPECTED DELIVERABLES

Virginia Tech will create an open API accessible to the CHREC community that can be used within an FPGA for analyzing and manipulating logic within the device. This work will leverage past work geared to the Xilinx V2Pro FPGA.

PROJECT BUDGET

This project is using three CHREC affiliate memberships.