

# EXECUTIVE SUMMARY

**PROJECT NAME:** V1-10 - On the Performance, Programmability, and Power of Accelerators

**INVESTIGATORS:** Wu Feng, Patrick Schaumont, Peter Athanas

## PROJECT DESCRIPTION

In recent years, a myriad of approaches have been proposed to tackle high-performance accelerator computing. The main contenders for such applications are multi-core CPU's, host-coupled GPU's and host-coupled FPGA's. Combining our experience in domain-specific application knowledge with platform-specific knowledge in FPGA and GPU, this project will perform a comprehensive characterization of the performance, energy-efficiency and power efficiency of high-end accelerators. The key contribution of this project is that a given set of application benchmarks will be simultaneously ported to multiple target platforms, thereby creating valuable insight into the suitability of each target platform for the selected application set. In addition, we will obtain insight into the relative performance of different target platforms against each other.

## EXPERIMENTAL PLAN

Task 1: A reference testbed environment for the performance evaluation of accelerators with respect to a multitude of performance metrics, both at the systems level and component level, e.g., inferring or directly measuring the power consumption, energy consumption, or energy efficiency of just the processor.

Task 2: A set of new performance metrics that can be feasibly measured or inferred at the entire systems level or at the individual component level, particularly processor.

Task 3: Portable and optimized application benchmark that is applied and evaluated on an FPGA and GPU platform.

## HOW THIS PROJECT IS DIFFERENT

The project leverages the expertise of design teams that are able to target complementary platforms (GPU and FPGA), while starting from the same reference specification. Therefore, we will strive to obtain the best possible performance using specialized design expertise for each platform.

## POTENTIAL MEMBER COMPANY BENEFITS

This will provide a reference testbed environment for the detailed characterization of emerging accelerators, most notably, the FPGA and GPU. By generalizing the characterization across devices, we expect to glean insights that enable applications to be better able to tap into the true potential of the emerging accelerator. In particular, the characterizations will be used to guide further optimizations for better performance, where performance is defined as speed, energy efficiency, cost, or productivity. In all, we seek to enable member companies to develop and deliver better products faster, with less risk and lower development costs.

## EXPECTED DELIVERABLES

Virginia Tech will create a blueprint for setting up a reference testbed environment for accelerators.

Using this testbed, we will generate a repository of performance characterizations and optimizations for the CHREC community that will be general enough to use across a set of emerging accelerators, in particular, FPGA and GPU. This work will leverage past CHREC work on traditional multicore, i.e., V2-08, where created an automated run-time system to improve process-to-core mappings to achieve better performance.

## PROJECT BUDGET

This project is using four CHREC affiliate memberships.

