

# EXECUTIVE SUMMARY

**PROJECT NAME:** V1-09 - Characterizing and Optimizing Emerging Devices

**INVESTIGATOR(S):** Wu Feng, Virginia Tech

## PROJECT DESCRIPTION

Systems that are based on accelerators, e.g., FPGA, reconfigurable multicore, GPGPU, and Cell, promise to deliver accelerated solutions to problems that might otherwise be intractable. However, these accelerators run into an array of issues when factors such as productivity, power, size, resiliency, and cost are considered. Building upon our expertise on parallelizing applications and characterizing multicore devices, we will further expand our application suite for device characterization across three accelerators: GPGPU, reconfigurable multicore, and traditional multicore (where spare cores are used as accelerators). More importantly, based on an analysis of this characterization, we aim to apply novel optimizations to speed-up the accelerated codes even further, e.g., a recent port of a long-range interaction code to the GPGPU produced a speed-up of 119x. Detailed profiling and analysis with NVIDIA's performance tools led to a series of hand-coded optimizations that improved overall performance by an additional 3x for an aggregate speed-up of 359x. In the longer term, we intend to automatically identify and codify such optimizations to enhance programmer productivity in such environments.

## EXPERIMENTAL PLAN

Task 1: Develop a suite of device-agnostic tests to evaluate and characterize emerging devices and their environments.

Task 2: Analyze the results of the above tests to guide system-level optimizations.

Task 3: Hand-optimize and tune codes on emerging devices with respect to a myriad of performance metrics, e.g., energy efficiency, speed-power ratio, and so on.

Risk exists in our ability to port the device-agnostic tests onto three different platforms.

## HOW THIS PROJECT IS DIFFERENT

Unlike other approaches that arguably only seek to *characterize* emerging devices, we intend to leverage the characterization to glean insight into how best to *optimize* our accelerator-based code for even better performance, where performance is defined as speed, energy efficiency, cost, or productivity.

## POTENTIAL MEMBER COMPANY BENEFITS

This will provide a detailed characterization of emerging devices as accelerators. By generalizing the characterization across devices, we expect to glean insights that enable a code developer to be better able to tap into the true potential of the emerging devices. In particular, the characterizations will be used to guide further optimizations for better performance, where performance is defined as speed, energy efficiency, cost, or productivity. In all, we seek to enable organizations to develop and deliver better products faster, with less risk and lower development costs.

## EXPECTED DELIVERABLES

Virginia Tech will create a repository of performance characterizations and optimizations for the CHREC community that will be general enough to use across a set of emerging devices, in particular, GPGPU, reconfigurable multicore, and traditional multicore. This work will leverage past CHREC work on traditional multicore, i.e., V2-08, where created an automated run-time system to improve process-to-core mappings to achieve better performance.

## PROJECT BUDGET

This project is using two CHREC affiliate membership.