

EXECUTIVE SUMMARY

PROJECT NAME: G8-10: PGAS Optimizations for Many-core Architectures

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PROJECT DESCRIPTION

Ease-of-use as a result of the global address space abstraction in PGAS coupled with its performance advantages due to locality awareness may help address escalating software complexity as a result of many-core architecture proliferation in HPC systems. With this belief, G8-09 project explored semantics of PGAS languages in general and UPC in particular on many-core architectures and delivered two prototype UPC compiler and runtime system implementations based on BUPC on Tile64 processor. One built over the GASNet pthreads conduit and the other over the GASNet MPI conduit. Performance analyses of these revealed specific optimization opportunities by closely mapping the compiler and runtime to the underlying many-core architecture. This project leverages and extends the G8-09 research successes and intends to further investigate these opportunities. As before we use the Unified Parallel C (UPC) as the PGAS language case study and the Tile64 processor as the target platform in our investigations. The optimizations being targeted fall under three general categories, namely, data and thread placement strategies, efficient use of on-chip networks for communication and collective operations, and addressing the address translation overheads in PGAS. During the course of this project we will investigate the impact of these optimizations on productivity using various application and benchmark case studies. Even though, the research carried out during this project will directly impact our UPC implementations on Tile64 processor, the concepts explored should be applicable to PGAS languages and many-core chips in general.

EXPERIMENTAL PLAN

The project is structured around three tasks:

Task 1: Explore optimized data and thread placement strategies.

Task 2: Investigate efficient use of on-chip networks for data transfer and collective operations.

Task 3: Explore optimizations for address translation overheads in PGAS languages.

HOW THIS PROJECT IS DIFFERENT

This project will result in the improved user productivity on many-core chips, and could therefore have a wide impact in the computing field in general. As one of the pioneers of the UPC language and developers of the GUTS (GWU UPC Testing Suite), the team is uniquely positioned to explore optimization opportunities and also propose their integration into the UPC compilers and runtime systems for higher productivity on many-core architectures. By our further investigations in providing this new programming model for Tiler's platform, this project complements earlier studies on TILE64 that involved performance evaluation and library implementations.

POTENTIAL MEMBER COMPANY BENEFITS

Many member benefits are expected from this project. The PGAS model study will provide insights on the many-core programming in general, and TILE64 programming in particular. Member companies will have influence over UPC application and benchmark selections to evaluate our optimizations. Members will also have first access to the resulting deliverables from this project. Through regular interactions, members will also be able to influence the extensions made to the UPC language. In the long run, it is expected that the extended UPC will become one of the primary means of programming many-core devices.

EXPECTED DELIVERABLES

The outcome of this project will include research papers on optimization concepts for PGAS languages on many-core architectures. The project will also deliver a prototype UPC compiler and runtime implementation that will facilitate the researched optimizations. Mid-term and final reports will document the research methods adopted, the progress of the project, as well as analyses and results obtained from the study.

PROJECT BUDGET

3 CHREC Memberships