

EXECUTIVE SUMMARY

PROJECT NAME: G8-09: Parallel Programming of Tilerla using Unified Parallel C

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PROJECT DESCRIPTION

Previous CHREC research has shown that the TILE64 multicore processor can complement FPGAs in high performance computing applications. With the availability of a large number of on-chip cores that are software programmable, the TILE64 platform promises a significant productivity advantage over FPGAs. This project intends to leverage this advantage and provide a programming model that will result in significant improvements to many-core programmability.

To achieve the desired objectives on Tilerla's platform, the Partitioned Global Address Space (PGAS) programming model is a very good candidate. PGAS provides programmers with a global address space which is logically partitioned, allowing threads to be aware of the locality of accessed data. Apart from the ease-of-use and data-locality awareness inherent in PGAS programming languages, the architecture of TILE64 exhibits interesting features for the PGAS model; for example, shared memory is available for each core, but locality is important due to the small size of the caches. In addition to memory access optimizations, there are other research challenges, such as exploiting fully all the available inter-core communication mechanisms.

During the course of this project, the platform from Tilerla will be first evaluated with respect to the PGAS programming model through a library integration study. A case study using the UPC language will be conducted and would lead to a prototype UPC compiler for the TILE64. Ultimately, it is expected that the research carried out during this project will result in UPC language improvements and new PGAS programming model concepts for many-core chips.

EXPERIMENTAL PLAN

The project is proposed to be carried out in the following stages:

- (a) Investigation of the Tile64 programming models
- (b) Library integration in UPC
- (c) Evaluation of the library integration approach
- (d) Study on UPC compiler requirements for Tilerla

HOW THIS PROJECT IS DIFFERENT

This project will result in the improved programmability of many-core chips, and could therefore have a wide impact in the computing field in general. As one of the pioneers of the UPC language, the team is uniquely positioned for proposing extensions to UPC for many-core chips. By providing a new programming model for Tilerla's platform, this project will complement earlier studies on TILE64 that involved performance evaluation and library implementations.

POTENTIAL MEMBER COMPANY BENEFITS

Many member benefits are expected from this project. The PGAS model study will provide insights on the many-core programming in general, and TILE64 programming in particular. With the addition of library support for the new Tilerla technology, it is expected that the project will also help reuse a vast amount of existing code when developing applications for TILE64. Through regular interactions, members will also be able to influence the extensions made to UPC language. In the long run, it is expected that the extended UPC will become one of the primary means of programming many-core devices.

EXPECTED DELIVERABLES

The outcome of this project will include a UPC compiler prototype, which will provide the PGAS model for programming many-core chips. Lessons learned during the course of the project, as well as techniques deployed for optimal usage of memory and communication resources in many-core chips, will be shared. Mid-term and final reports will document the research methods adopted, the progress of the project, as well as analyses and results obtained from the study. It is also expected that a couple of papers will be published in journals and conferences.

PROJECT BUDGET

3 CHREC Memberships