

## EXECUTIVE SUMMARY

**PROJECT NAME:** G7-10: Hardware Virtualization: System Level Support for HPRCs

**INVESTIGATOR(S):** Dr. Tarek El-Ghazawi, GWU site of CHREC

### PROJECT DESCRIPTION

High performance reconfigurable computers (HPRCs) are characterized by the multiplicity in FPGAs as well as an imbalance in the number of microprocessors and FPGAs, making it a challenge for parallel applications to achieve the best possible utilization of the available hardware resources, while at the same time maintaining portability across HPRCs. With the advent of multi-core technology, efficient hardware utilization is a greater challenge, because the increased microprocessor components can lead to a large number of software processes sharing the available reconfigurable hardware. Since software processes can originate from either the same parallel application, different applications or even from different users, a compile-time prediction of the run-time execution scenario is not possible. A centralized, system-level run-time support is therefore essential in order to efficiently manage the hardware resources in a transparent manner, in addition to providing the developer with an abstraction that hides the details of multiplicity of FPGAs, scheduling techniques, node architecture, and hardware implementation.

In this project, we propose a system-level resource virtualization solution that is based on run-time reconfiguration of FPGAs at the hardware level, and kernel-space based resource management on the software side. Building on the results of G7-09, and using the lessons learnt from the initial virtualization prototype built in the user-space, the G7-10 project will focus on incorporating an efficient system-level virtualization support into the operating system, complemented by a software stack that will provide access to the available services at a suitable level of abstraction. The developed solution will be optimized in order to minimize the overheads due to the virtualization layer.

### EXPERIMENTAL PLAN

The proposed system-level solution will be composed of the following stages of development:

- (a) *API specification:* Develop a simple API for accessing hardware resources in HPRCs. Based on hardware tasks defined in a centralized library, this API will allow users to accelerate relevant parts of their application by using software function calls. The underlying resource management details will be hidden from the user.
- (b) *Support for managing virtual resources in the kernel-space:* Investigate and develop an efficient virtualizer within the OS for managing the available hardware resources. This component will cater to requests for hardware tasks and virtual resources from multiple processes, and appropriately schedule them on physical resources. Kernel-level optimizations will allow efficient operation of FPGA configuration and data transfer, incurring minimum overheads from the virtualization manager.
- (c) *Run-time system:* Provide an efficient software stack for accessing the reconfigurable resources using the defined API. The run-time system will be responsible for translating the API calls into the desired sequence of accesses to the machine-specific virtualization manager. The run-time system will also provide access to the hardware task library.
- (d) *Evaluation methodology:* Research and develop a methodology for evaluating the proposed virtualization solution. The developed infrastructure will exercise the system with some sample application tasks, to obtain performance measurements for a prototype virtualization solution on Cray XD1.

### HOW THIS PROJECT IS DIFFERENT

This project will provide one of the first system-level support solutions for virtualization of reconfigurable resources in high performance reconfigurable computers. This will allow easier application development, in addition to efficient use of the reconfigurable resources. The developed solution may be used by others as a model or reference for developing similar systems for their HPRC machines. The proposed solution will also position us to extend it for heterogeneous compute resources, which has the potential of far reaching impact.

### POTENTIAL MEMBER COMPANY BENEFITS

- Member companies will have access to one of the first system-level tools for virtualizing FPGA resources in an HPRC.
- In addition to the virtualizing software, members will be able to directly use the provided examples and evaluation methodologies for benchmarking their systems.
- Member organizations will also be able to influence the project direction by providing valuable feedback.

### EXPECTED DELIVERABLES

- System level software for virtualizing FPGA resources on the Cray XD1. This will include the kernel modules, supporting libraries and run-time system, as well as usage examples.
- Several conference and journal publications arising out of the proposed research.

### PROJECT BUDGET

2 CHREC Memberships