

EXECUTIVE SUMMARY

PROJECT NAME: F6-11 – Adaptive Space Computing

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PROJECT DESCRIPTION

The requirements of advanced computing systems for space as well as other high-performance embedded computing (HPEC) systems differ from traditional computing systems. While high performance is obviously desired, other factors such as reliability and power consumption can be even more important. Addressing all of these factors while minimizing cost is a significant challenge, especially as processing requirements of future systems continue to scale higher. Commercial-off-the-shelf (COTS) microprocessors, FPGAs, and other fixed- or reconfigurable-logic, multi/many-core devices can provide required performance at a significantly reduced cost, but at the expense of less radiation-tolerant and reliable components.

This project is investigating and enhancing COTS-based, fault-tolerant (FT) system architectures based upon a variety of software and hardware techniques, with emphasis upon system-level fault tolerance and testing. Our concept of reconfigurable fault tolerance (RFT) exploits the ability of each FPGA to partially reconfigure itself while in operation, changing modes of fault tolerance concomitant with changes in radiation hazards, allowing real-time adaptation to environmental factors that may affect system reliability while avoiding the low performance of worst-case-scenario designs. By modifying the amount of redundant logic within one FPGA or a set of FPGAs, systems can dynamically tradeoff reliability and performance.

With our dependability infrastructure (DI) concept, we explore adapting and extending system-level, software-implemented fault tolerance or SIFT to many-core devices (e.g. TILE64, Maestro) and reconfigurable devices (e.g. Virtex, SIRF), as well as complex, distributed, heterogeneous systems such as satellite constellations. The focus of the study is exploration of adaptive middleware enabling reliable network communication and distributed job management.

To validate results from a variety of fault detection and mitigation methods, we require testing tools able to reach across multiple systems. Our concept of fault injection (FI) for space systems, encompassing both temporal and spatial aspects of FI using our Simple Portable Fault Injector (SPFI), exploits a variety of debugging and programming techniques available for FPGA and microprocessor-based systems to form a portable FI framework that can target various devices.

EXPERIMENTAL PLAN

RFT was originally introduced in CHREC project F4-08 as a proof-of-concept for partial reconfiguration (PR) in space, and extended to provide multiple FT modes (e.g. unprotected, self-checking pair (SCP), triple-modular redundancy (TMR), algorithm-based fault tolerance (ABFT)) in F6-09. F6-10 further augmented the RFT framework to provide FPGA services for state saving and recovery with hardware checkpointing and rollback techniques on FPGA systems. F6-11 will develop research ideas and tools for easily creating RFT systems by integrating automation capabilities into the VAPRES system builder tool for PR from CHREC project F4-10. Additionally, an RFT interface for the Dependability Infrastructure middleware task will enable FPGA-based space systems to connect to larger DI-based systems.

Techniques from our team's experience leading R&D on the NASA Dependable Multiprocessor project will be adapted to many-core and reconfigurable architectures, using TILE64, ML-501, and (when available) Maestro boards as prototype platforms. A variety of architecture choices will be explored, including task and hardware granularity and network communication protocols, in order to develop a flexible software infrastructure allowing unreliable COTS components to be integrated together for reliability and high-performance.

A task on FI for space systems will explore methodologies and procedures for combining FI methods to evaluate susceptibility of space systems which comprise of FPGAs, traditional CPUs, and emerging many-core devices. The SPFI concept and tool were introduced in CHREC project F6-09 and refined in F6-10. F6-11 will further expand SPFI with concepts for temporal FI on FPGAs to explore time dependency of the FI process. In addition, use of special FI methods, developed for FPGAs, will be explored to enable faster fault injection on multicore systems.

HOW THIS PROJECT IS DIFFERENT

While many research groups have studied FT strategies and mechanisms for FPGAs (e.g. scrubbing and TMR), this project is unique in its focus upon adaptive fault tolerance for dynamic tradeoffs between performance and reliability. Our focus is upon several levels, such as the system level with SIFT methods and the device level with hardware reconfiguration. Similarly, although fault injection has garnered much attention in the field, SPFI is unique in its comprehensive ability to target heterogeneous types and sets of devices and do so spatially and (soon) temporally.

POTENTIAL MEMBER COMPANY BENEFITS

- Influence over project direction, ensuring relevance to interesting systems, applications, and problems
- Access to research exploring novel ways to achieve performance and dependability in space-based processing

EXPECTED DELIVERABLES

- Prototypes of dependable middleware and fault-injection services for systems with varying architectures
- RFT system builder tool allowing for automated creation of RFT systems
- Several scholarly conference and/or journal publications

PROJECT BUDGET: 3 memberships