EXECUTIVE SUMMARY

PROJECT NAME: F6-09: Reconfigurable & Hybrid Fault Tolerance

INVESTIGATOR(S): Dr. Alan D. George & Dr. Ann Gordon-Ross, Univ. of Florida site of CHREC

PROJECT DESCRIPTION

The requirements of advanced computing systems for space as well as other high-performance embedded computing (HPEC) systems differ from traditional HPC systems. While high performance is obviously desired, other factors such as reliability and power consumption can be even more important. Meeting all of these factors while minimizing cost is a significant challenge, especially as the processing requirements of future systems continue to scale higher. Commercial-off-the-shelf (COTS) microprocessors, FPGAs, and other fixed or reconfigurable multicore devices can provide the required performance at a significantly reduced cost, but at the expense of less radiation-tolerant and reliable components.

This project will investigate and enhance COTS-based, fault-tolerant system architectures based upon a variety of software and hardware techniques, with an emphasis upon system-level fault tolerance. Our concept of reconfigurable fault tolerance (RFT) exploits the ability of each FPGA to partially reconfigure itself while in operation, changing modes of fault tolerance concomitant with changes in radiation hazards, allowing real-time adaptation to environmental factors that may affect system reliability while avoiding the low performance of worst-case-scenario designs. By modifying the amount of redundant logic within one FPGA or a set of FPGAs, systems can dynamically tradeoff reliability for increased performance. Our concept of hybrid fault tolerance (HFT) examines many different FT strategies (hardware- and software-based) in order to develop a system-level framework to spatially mix control-flow and data-flow methods for better coverage with less overhead. Since each method has unique strengths and weaknesses, it is important to understand how to combine these methods effectively. Additionally, this project will explore the FT characteristics of several new RC devices, such as Tilera Tile64, Achronix Speedster, and Xilinx SIRF.

EXPERIMENTAL PLAN

RFT was originally introduced in CHREC project F4-08 as a proof-of-concept for partial reconfiguration, with a few FT modes (unprotected, self-checking pair (SCP), or triple-modular redundancy (TMR)). F6-09 will extend the RFT analytical methodology to include additional modes, such as algorithm-based fault tolerance (ABFT), which have the potential to increase reliability with very little overhead. RFT will also be extended to allow modeling of power consumption vs. reliability.

The HFT task will explore methodologies and procedures for combining FT methods effectively for system-level protection. A system-level FT framework for HFT will be created which combines varying hardware and software-based FT methods as well as provides strategies for combining and transitioning between methods while maintaining maximum reliability. Software and hardware techniques (code transformation/ABFT/architectural enhancements) will be used to protect soft-core processors running on FPGAs.

Additionally, this project will develop one or more vulnerability metrics for FPGAs and other RC devices in order to evaluate the susceptibility of these devices to errors. By assessing the vulnerability of these devices, system designers can devise appropriate fault-tolerance schemes for their specific applications/missions.

HOW THIS PROJECT IS DIFFERENT

While many other research groups have studied fault-tolerant approaches for FPGAs (scrubbing and TMR), we believe that RFT is the first project studying the use of real-time adaptive fault tolerance with partial reconfiguration.

The HFT project leverages previous work in fault-tolerant systems, such as the NASA Dependable Multiprocessor developed by Honeywell and the University of Florida, which pioneered and featured a fault-tolerant software framework to mitigate COTS radiation susceptibility for a suite of FT modes and space-based applications for a space supercomputer.

POTENTIAL MEMBER COMPANY BENEFITS

- Influence over project direction, ensuring relevance to interesting systems, applications, and problems
- Access to research exploring novel ways to provide fault tolerance in FPGAs and RC systems

EXPECTED DELIVERABLES

- RFT prototype platform implemented on a Xilinx ML401
- HFT framework and any supporting software tools
- Several scholarly conference and/or journal publications

PROJECT BUDGET: 3.5 memberships