

EXECUTIVE SUMMARY

PROJECT NAME: F5-10, Device/Application Mappings - Measurement, Performance, and Prediction

INVESTIGATOR(S): Dr. Alan George & Dr. Herman Lam, UF site of CHREC

PROJECT DESCRIPTION:

The goal of this project is to develop a fundamental research foundation to explore Reconfigurable Computing (RC) devices and their relationships to applications and achievable utilization. The primary motivation for this work is to gain insight on device suitability for a variety of application requirements. New research will define application metrics that relate to device characterization to establish a mapping between the device and application domains. Developing the mapping between the device and application domains will enable application performance prediction on existing and notional devices without requiring the implementation of test code on the target platform. Additionally, previous device characterizations at CHREC focusing upon computational performance, power consumption, and memory limitations, as well as new device characterizations such as I/O limitations and radiation tolerance, will be extended to new architectures such as the Achronix Speedster, Coherent Logix HyperX, Abound Raptor, and several additional fixed-logic multicore devices. Achievable utilization on devices and systems that use these devices will also be studied to explore the discrepancies between observed and theoretical performance and how unique features and tools can enhance their performance.

EXPERIMENTAL PLAN:

This project has two major tasks: device & application studies and achievable utilization studies. The device characterization task will leverage techniques from previous F5 research to perform an in-depth architectural analysis of emerging RC technologies by applying the computational density (CD), computational density per Watt (CD/W), internal memory bandwidth (IMB), and external memory bandwidth (EMB) metrics defined in our prior publications and presentations to new devices. The CD and CD/W metrics will be augmented to allow for user-controlled parameters (such as operation types), and an I/O bandwidth metric will be created with the goal of characterizing a device's ability to receive and send data to or from the chip. Insights gained in the device characterization task can be used for a notional redesign of existing architectures. The CD and CD/W metrics will also be used together with the radiation tolerance of devices to determine their capability to perform in space when fault-tolerance is a necessity. Several metrics to describe algorithm parallelism and memory requirements will also be studied. Application parallelism and memory demand can then be mapped to device parallelism capability and bandwidth to project application performance on various existing and notional devices.

The achievable utilization task will strive to understand the utilization limited by a user's ability to access hardware capabilities of a device and the limitation by subsystems that surround a device. Previous F5 application and kernel case studies, as well as new kernel studies and literature searches, will be used to better understand and estimate achievable device utilization. These case studies will be used to observe CD's ability to represent and predict a device's strengths and weaknesses. Device utilization limited by the system or subsystems that surround a device, such as the board, interface, memory, or middleware, will also be evaluated. In addition, RC devices will be compared to fixed-logic multi/manycore devices to see if there are inherent differences in achievable utilization.

HOW THIS PROJECT IS DIFFERENT:

This project differs from previous work by expanding beyond device characteristics to explore application characteristics and the relationships between application metrics and device metrics, especially with reference to power. This project will focus upon analyzing the ideal mix of device characteristics needed to maximize application performance. Insights gained during device analysis allow for the study of notional architecture improvements, and the application to device mapping studies provide a framework to examine the impact of these improvements. This project emphasizes the growing importance of power in device studies and performance in radiation environments. Device metrics account for power consumed to help reveal devices that are power-efficient.

POTENTIAL MEMBER COMPANY BENEFITS:

Member companies will be able to benefit from each of the tasks in different ways. From Task 1, members will be able to observe and exploit for their needs these comparisons of new device technologies in a fair and level arena based upon the device metrics developed. Members will also be able to observe and evaluate how applications can be characterized in order for comparison to device features and characteristics. From Task 2, member companies will be able to ascertain how much performance a user is able to realistically achieve from devices as well as identify bottlenecks that limit a device's capabilities in a system. These two tasks will work together to aid member companies in making strategic research and development decisions allowing for more time and research efficiency.

EXPECTED DELIVERABLES:

- Midterm and final reports documenting research methods, progress, results, and analysis of each task
- Application/device projection model; characterizations of new devices; utilization studies
- Several scholarly conference and/or journal publications

PROJECT BUDGET:

- Funding for this project is ~5 memberships.