EXECUTIVE SUMMARY

PROJECT NAME: F4-10, PR Architecture and Design Toolset for Embedded and Aerospace Systems

INVESTIGATOR(S): Dr. Ann Gordon-Ross & Dr. Alan George, UF site of CHREC

PROJECT DESCRIPTION

This project consists of three main tasks. The first task implements, verifies, and evaluates our novel **V**irtual **A**rchitecture for rapid system development, prototyping and flexible system operation of **P**artially **R**econfigurable **E**mbedded **S**ystems (VAPRES). VAPRES was initially proposed in F4-09 to assist in efficient PR design. It provides a generalized PR floorplan by prepartitioning the FPGA into several PR regions (PRRs). Using VAPRES, designers partition applications into communicating modules and map these modules to the predefined PRRs. Deliverables include a builder tool that automates the process of creating a VAPRES-based system, eliminating time-costly and error-prone steps such as specialized PR floorplanning. Additional deliverables include scripts and programs for automating application development for the VAPRES system. Automatable steps include task-graph generation and partitioning to identify the design's task/module flow and dependencies for module-to-PRR scheduling and mapping.

The second task is to augment the VAPRES system with capabilities to assist space-based sensor network development. Deliverables include the development of a runtime manager for online scheduling and placement of hardware modules inside VAPRES PRRs. Necessary runtime manager capabilities include context passing to assist mobile nodes tracking stationary targets (i.e. process migration between nodes) and embedded bitstream relocation. Bitstream relocation enables a partial bitstream compiled for placement in a specific PRR to be placed in a different PRR, eliminating the need for multiple redundant bitstreams. Additional deliverables include integrating the VAPRES runtime manager as a kernel module in a soft-core processor operating system for hardware multi-threading. This approach allows multiple applications to concurrently execute and access VAPRES architectural features.

The third task architects models and methodologies for capturing and analyzing formal application specifications to derive PR architecture. Formal application specifications include UML models, CDFGs, and data flow graphs. This task will explore automatic generation and evaluation of potential PR architectures via PR amenable block identification and PR-oriented hardware/software partitioning. While retaining the original design specification, automatic generation and evaluation of PR architectures will enable design metric evaluation such as reconfiguration and area overhead and the impact of the design floorplan/layout on the application performance.

EXPERIMENTAL PLAN

VAPRES was originally introduced in F4-09 as a proof-of-concept for embedded partial reconfiguration. F4-10 will enhance the builder tool from F4-09 by adding new features such as full inter-module communication (using MACS, an underlying streaming NoC developed in F4-09) and support for Virtex-5 devices. Additional VAPRES builder tool enhancements include back-end migration to the Xilinx ISE V11 tool suite and GUI refinement to provide a full IDE (integrated development environment) for PR embedded system development. VAPRES performance (e.g. dynamic power consumption and partial reconfiguration times) will be evaluated for different VAPRES designs, each design using a different set of architectural parameters. In addition, we will develop a complete VAPRES API and runtime manager, create methods to save and restore the context of hardware modules, and architect a seamless module migration methodology. This approach would allow moving hardware modules to different FPGAs without data stream processing interruption. Finally, we will integrate the runtime manager into an embedded operating system.

HOW THIS PROJECT IS DIFFERENT

The study of PR formulation has not yet been explored by our group. In addition to this, the level of PR automation we are studying is far more extensive than it was in 2009.

With VAPRES, we are taking previously isolated research such as bitstream relocation, and incorporating them into VAPRES to increase robustness, usability and flexibility. We are then using it as a base to explore new applications, more power-efficient PR usage and runtime system adaptability.

POTENTIAL MEMBER COMPANY BENEFITS

- Access to the VAPRES builder tool, API, and embedded bitstream relocation
- Access to context save-and-restore methodologies
- Access to PR design automation scripts
- Evaluation, feedback, and requirement specifications to drive project task directions

EXPECTED DELIVERABLES

- VAPRES builder tool for the ML401 (Virtex-4) and ML509 (Virtex-5) boards
- API and runtime manager for VAPRES
- Live target-tracking demo using the VAPRES system
- Several scholarly conference and/or journal publications

PROJECT BUDGET

- 3 memberships