EXECUTIVE SUMMARY

PROJECT NAME: F4-09: Virtual Architecture and Design Automation for Partial Reconfiguration

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PROJECT DESCRIPTION

The first task in F4-09 is to architect a **V**irtual **A**rchitecture for rapid system development and prototyping and flexible system operation of **P**artially **R**econfigurable **E**mbedded **S**ystems (VAPRES) to ease the use of partial reconfiguration (PR), since efficient PR use is a highly specialized task. VAPRES provides a generalized PR floorplan by pre-partitioning the FPGA into several PR regions (PRRs). Using VAPRES, designers only partition applications into communicating modules and map these modules to the predefined PRRs. VAPRES eliminates time-costly steps such as specialized PR floorplanning and reduces synthesis times. VAPRES enables flexible system operation, since VAPRES provides an architecture in which applications may time-multiplex PRRs using an on-board controlling agent (residing in the FPGA's static region) to dynamically place and schedule application modules to the predefined PRRs.

The second task in F4-09 is to develop a suite of software tools for PR design automation to further ease PR development for system designers. Our software tools will consist of scripts and programs intended to augment the current Xilinx Early Access Partial Reconfiguration tools. Automatable steps include PR design creation, task-graph partitioning for application module extraction, application module mapping to PRRs, reconfiguration scheduling, and floorplan/layout generation.

EXPERIMENTAL PLAN

VAPRES requires both architectural development and systems research as well as operational research. Architectural development and systems research includes architecting, implementing, testing, and evaluating an efficient PRR communication architecture using SCORES – a **S**treams-based **CO**mmunication A**R**chitecture for **E**mbedded **S**ystems. SCORES provides dynamic communication establishment between arbitrary PRRs. VAPRES and SCORES will be architected, implemented, and evaluated using a Xilinx ML401 prototyping board. A VAPRES bitstream relocation agent will orchestrate dynamic module state saving and relocation. Operational research includes designing and evaluating custom algorithms for dynamic module placement, scheduling, and module preemption.

PR design automation requires specifying VHDL programming constructs and directives for application developers and associated VHDL parsing tools. Our PR design automation plan involves a bottom-up approach, initially providing application developers with automated low-level PR support (such as PRR sizing and placement), and then building on these low-level supports with automated high-level PR support (such as automated application module overlaying and module extraction).

HOW THIS PROJECT IS DIFFERENT

PR design is a highly-specialized and time consuming task, requiring specialized system knowledge and expertise in a variety of areas. PR designers not only must develop a functioning application, but they must also architect an efficient PR layout for that application. F4-09 will enhance existing PR systems research by providing new design techniques and automation tools and methodologies to provide fundamental support to PR system designers.

POTENTIAL MEMBER COMPANY BENEFITS

- Access to the VAPRES base platform and development tools
- Access to the scripts for PR design automation
- Evaluation, feedback, and requirement specifications to drive project task directions

EXPECTED DELIVERABLES

- VAPRES base platform prototype implemented on a Xilinx ML401 board
- VAPRES and SCORES architecture performance
- PR design automation software suite (scripts and programs)
- Several scholarly conference and/or journal publications

PROJECT BUDGET

- 3 memberships