

EXECUTIVE SUMMARY

PROJECT NAME: F2-10, Hardware Virtualization Layer for Ubiquitous RC

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PROJECT DESCRIPTION

The goal of this project is to start to address several of the key challenges preventing the mainstream use of RC, including the current requirement for specialized RC languages, lengthy place-and-route times and high memory footprint, and an arduous verification and optimization cycle. By addressing these challenges, RC applications can be developed in a similar manner to those for GPUs or other heterogeneous, parallel systems, significantly expanding the potential scope for employing RC devices.

To remove the requirement of a specialized RC language, this project will investigate the feasibility of OpenCL synthesis, specifically addressing the conversion of OpenCL memory accesses into more efficient stream accesses on an FPGA. In addition, while our Intermediate Fabrics (IF) concept has demonstrated place-and-route speedups of two orders of magnitude, significant area overhead can be incurred. This project addresses this overhead by investigating hard-IFs, where physical routing resources on the FPGA are used rather than register-transfer-level resources. Finally, bottleneck visualizations and automatic analysis concepts are researched for high-level synthesis (HLS) languages, providing significant acceleration to the optimization process.

EXPERIMENTAL PLAN

Intermediate Fabrics:

- Investigate strategies to minimize timing/area overhead and improve flexibility of Intermediate Fabrics (IFs) by mapping virtual routing resources and functional units directly onto physical resources.
- Investigate OpenCL high-level synthesis techniques for converting SIMD memory requests into data streams.

Performance Analysis:

- Expand current Reconfigurable Computing Application Performance (ReCAP) framework and tool developed at CHREC to include bottleneck visualizations and expanded bottleneck visualizations for HLS-based RC applications.

HOW THIS PROJECT IS DIFFERENT

OpenCL: To our knowledge, this project is the first to investigate high-level synthesis from OpenCL code onto FPGAs.

Intermediate Fabrics: Previous work (e.g., QUKU) has implemented a coarse-grained reconfigurable architecture specialized for DSP applications on top of an FPGA, with the goal of providing fast partial reconfiguration for DSP applications. Our project focuses on minimizing PAR times and the development of a more complete understanding of generic reconfigurable fabrics implemented atop FPGAs, including development of tools supporting these architectures.

Performance Analysis: Current performance analysis tools for microprocessors support automated analysis and visualization; however they lack support for FPGAs. To our knowledge, no framework or tool exists that provides bottleneck visualization and automatic analysis for HLS-based RC applications.

POTENTIAL MEMBER COMPANY BENEFITS

Access to tools to explore the implementation of coarse-grained and application-specific reconfigurable architectures on FPGAs, tools integrated with vendor toolkits for the implementation of designs on Intermediate Fabrics (which has the potential to significantly reduce PAR times), and performance tools that can significantly improve the productivity of implementing a correct and high-performing RC application (even in a large-scale system).

EXPECTED DELIVERABLES

- Tools for generating IFs and associated PAR tools as well as ReCAP with automated analysis and visualization.
- Several conference or journal publications containing project research and results.

PROJECT BUDGET: 2.5 memberships.