

EXECUTIVE SUMMARY

PROJECT NAME: F2-09: Translation and Execution Productivity

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PROJECT DESCRIPTION

The goal of this project is to improve translation and execution productivity for FPGA-based applications via three major improvements to the FPGA design flow: performance analysis techniques for automatic analysis, rapid placement & routing (PAR), and in-circuit debugging. The goal of automated analysis is to reduce the expertise and effort needed to optimize an RC application by automatically determining what to monitor, what constitutes a bottleneck, and what potential optimizations may remedy a given bottleneck. By providing automated analysis for RC applications, along with performance prediction and optimization strategies based upon acquired performance data, the amount of time spent optimizing an RC application can be drastically reduced.

To reduce lengthy PAR times that now commonly range from hours to even days, this project will investigate virtual PAR-specialized reconfigurable fabrics that act as an intermediate translation layer (referred to as *Intermediate Fabrics*) between a netlist and underlying physical device. Intermediate Fabrics enable rapid PAR (preliminary results show >100x speedup) for commercial-off-the-shelf devices, which provides rapid in-circuit debugging in addition to portability across devices. This project also addresses the considerable difficulty associated with in-circuit debugging for large-scale RC applications, focusing on applying assertion-based techniques on-chip at runtime. Using this infrastructure, an assert can be employed at runtime (not just in simulation), providing critical error information (e.g., node, condition, related data).

EXPERIMENTAL PLAN

Performance Analysis:

- Expand current Reconfigurable Computing Application Performance (ReCAP) framework and tool developed at CHREC to include automated bottleneck detection for HLL-based RC applications.
- Research more targeted optimization strategies, better automated analysis techniques, and potential use of performance prediction to accelerate the performance analysis process for HDL-based RC applications.

Intermediate Fabrics:

- Explore timing/area overhead and flexibility of Intermediate Fabrics (IFs) by implementing existing application-specialized reconfigurable architectures as IFs.
- Investigate strategies to minimize overhead based upon factors identified in this exploration.

Debug:

- Leverage performance analysis infrastructure to enable in-circuit assertion-based verification by synthesizing hardware-based asserts in both HDL-based and HLL-based RC applications.
- Trace data relevant to assert failure (node, related hardware signals, etc.) to facilitate rapid debugging.

HOW THIS PROJECT IS DIFFERENT

Performance Analysis: To our knowledge, no performance analysis tool or framework exists that provides automated bottleneck detection for HLL-based RC applications, nor for suggesting optimizations for HDL-based RC applications.

Intermediate Fabrics: Previous work (e.g., QUKU) has implemented a coarse-grained reconfigurable architecture specialized for DSP applications on top of an FPGA, with the goal of providing fast partial reconfiguration for DSP applications. Our project focuses on minimizing PAR times and the development of a more complete understanding of generic reconfigurable fabrics implemented atop FPGAs, including development of tools supporting these architectures.

Debug: FPGA debugging in this field currently focuses on a single FPGA and not on the entire system, thus making existing strategies less suited for debugging RC applications that employ multiple FPGAs. While "asserts" and other debugging constructs are used in simulation, these typically are not synthesized, reducing their use and effectiveness. This project seeks to remedy both of these shortcomings.

POTENTIAL MEMBER COMPANY BENEFITS

Access to tools to explore the implementation of coarse-grained and application-specific reconfigurable architectures on FPGAs, tools integrated with vendor toolkits for the implementation of designs against Intermediate Fabrics (which has the potential to significantly reduce PAR times), and debug and performance tools that can significantly improve the productivity of implementing a correct and high-performing RC application (even in a large-scale system).

EXPECTED DELIVERABLES

- Tools for generating IFs and associated PAR tools as well as ReCAP with automated analysis and debug support.
- Several conference or journal publications containing project research and results.

PROJECT BUDGET: Three memberships.

