

EXECUTIVE SUMMARY

PROJECT NAME: F1-09: System-Level Formulation and Design

INVESTIGATOR(S): Drs. Alan George, Herman Lam, & Greg Stitt, U. of Florida site of CHREC

PROJECT DESCRIPTION:

This project group focuses on analyzing challenges and limitations inherent in current methods of system-level application development on FPGA-based and other RC systems. Different methods for improving developer productivity have been identified and proposed solutions are demonstrated via development and evaluation of novel tools.

One part of this project is investigating methodologies for planning and analysis of parallel applications for RC to ensure time- and cost-effective solutions, a process we call *formulation*. Specifically, research methods are explored for automated strategic design-space exploration (DSE) in RC, by proposing and evaluating models and algorithms for automated mapping of RC applications described using an abstract modeling language previously created by our group called RCML. Research also includes expansion of our previously developed analytic performance prediction model known as RAT to support performance prediction of multi-FPGA and other related multi-device systems, in order to evaluate system mappings proposed by automated DSE tools in an integrated environment.

The second part focuses upon research, design, and evaluation of a coordination framework for heterogeneous application development. We define and analyze a single standardized framework based upon both a message-passing model and a simplified shared-memory, partitioned global-address-space (PGAS) model, along with concomitant APIs, allowing tasks on heterogeneous devices to communicate and coordinate, methods that can potentially be used with any heterogeneous platform.

EXPERIMENTAL PLAN

For one part of the project, to research automated DSE in RC, we begin with a literature survey of existing models and algorithms for automated scheduling of parallel applications. From that survey, we identify existing and propose new models and algorithms that will support automated mapping/scheduling for RC applications. We implement and evaluate selected techniques and integrate with a new multi-FPGA analysis tool within our abstract modeling environment called RCML. We evaluate automated DSE techniques using several RCML models as case studies.

In the second part, we study existing approaches for developing heterogeneous applications. From that basis, we define a framework and API for system-level coordination, then develop and evaluate a prototype System Coordination Framework (SCF, with associated libraries, compilers, etc.) and demonstrate its utility by supporting a few selected platforms as proof-of-concept case studies. Included in this part, we also study methods to bridge between the fields and tools of HPC and RC, programming and execution, in terms of SHMEM, a library based upon a simple PGAS programming model, one which provides low-latency, high-bandwidth, one-sided communications. In so doing, low-level programming concepts, models, and tools generally employed by device-level RC programmers will be adapted to mate with the coordination model of SHMEM for what is hoped will be a simple and highly efficient methodology for reconfigurable HPC.

HOW THIS PROJECT IS DIFFERENT:

Past research is non-existent in modeling of parallel applications on heterogeneous systems comprised of FPGAs for automated mapping and scheduling. Existing techniques typically assume homogeneous execution platforms. No other projects are tackling this problem as a tool for early RC design-space exploration.

Programming languages for device-level design for RC devices have received tremendous attention, and have evolved to raise the level of abstraction visible to the developer. However, programming such systems is still difficult and time-consuming. This work attempts to create a design-automation framework that creates customized communication for applications in such systems. Much of the past research on coordinating computational resources has been focused upon homogeneous sets of devices. This work attempts to address several challenges associated in coordinating heterogeneous devices in a general way that can be applied to a large spectrum of heterogeneous platforms.

POTENTIAL MEMBER COMPANY BENEFITS:

- Access/influence w/ expanded suite of RC formulation tools, including RC Modeling Language (RCML) editor with automated mapping/DSE and multi-FPGA RAT tools, and RC Simulation Environment (RCSE)
- Access/ influence w/ preliminary SCF and associated library and tools

EXPECTED DELIVERABLES:

- Expanded RCML editor, including automated DSE capabilities built-in and multi-FPGA RAT analysis tool
- SCF along with its associated tools and support for implementation on preliminary systems
- Several scholarly conference or journal publications

PROJECT BUDGET: 3 memberships