CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B6-11: FPGA Reliability*

INVESTIGATOR(S) *Mike Wirthlin, Brent Nelson*

PROJECT DESCRIPTION:

Previous work has focused on the use of reconfigurable devices in space-based systems, specifically in the areas of: **reliable clock domain crossing**, **soft-core processor reliability, reduced cost mitigation techniques, and reliable high-speed serial I/O**. In this project we continue that work on a number of fronts: fault-tolerant soft-core processor design, reliable BRAMs for SIRF designs, half-latch detection for Virtex-5 and Virtex-5QV FPGAs, and reliable serial I/O.

EXPERIMENTAL PLAN:

Fault-tolerant soft-core processor: 1) Create library of FT soft-core LEON3 processors including multi-core techniques 2) provide probability modeling for reliability techniques 3) perform ion beam radiation testing of these techniques to gather data on their performance.

Reliable Serial I/O: Perform ion accelerator beam testing of a variety of B1-10 serial I/O designs in conjunction with the XRTC organization. The first will be a basic Aurora test using multiple channels. Follow-up tests will focus on mitigated designs created in B1-10 consisting of redundant channel and retransmit architectures.

Reliable BRAM Data Storage: Create test designs of alternate BRAM mitigation techniques for use in both Virtex-5 and Virtex-5QV parts. Create analytical models to describe the reliability of general memories, memories used as FIFOs, and memories with non-uniform write rates. Perform ion accelerator beam testing of these designs to ascertain failure rates, failure mechanisms, and the efficacy of both the built-in ECC as well as custom-designed ECC mechanisms for recovery.

Half-Latch Detection: Create a Java and XDL-based tool to detect half-latches in Virtex-5 and Virtex-5QV designs, identifying the specific location of half-latches existing in those designs.

HOW THIS PROJECT IS DIFFERENT:

Existing processors in space are slow and very expensive, since they must be radiation hardened. This project will allow soft-core processors to be used in space reliably without the need for radiation hardening. Also, the reliability of serial I/O communications and BRAMs is not currently well understood – this project will contribute crucial understanding regarding their failure mechanisms, fault probabilities, and the recovery mechanisms which may be employed when failures do occur. In addition, it will produce both analytical models and a variety of real-life example designs which have been ion beam tested.

POTENTIAL MEMBER COMPANY BENEFITS:

This year's work will provide important data which will enable our members to understand when and how best to mitigate designs involving soft-core CPUs, BRAMs, and high speed serial links against upsets in harsh radiation environments. It will also help them better analyze the reliability of their existing FPGA designs with respect to half-latches. Finally, it will provide them a collection of sample designs to illustrate the tradeoffs involved.

EXPECTED DELIVERABLES:

1. A library of fault-tolerant LEON3 processors
2. Novel fault-tolerant techniques for softcore processors
3. Probability modeling for processor fault-tolerant techniques
4. Example designs for reliable serial I/O based communication and BRAM based data
5. Radiation test results for all of the above.
6. Technical papers and project reports on the above.

PROJECT BUDGET: Four memberships

GRADUATE STUDENT PROJECT LEADERS: Nathan Rollins and Kevin Ellsworth