# CHREC PROJECT EXECUTIVE SUMMARY

**PROJECT NAME** *B6-10: Reliable Architectures for Reconfigurable Computing*

**INVESTIGATOR(S)** *Brent Nelson, Mike Wirthlin*

## PROJECT DESCRIPTION:

Previous work has focused on the use of reconfigurable devices in space-based systems, specifically in the areas of **reliabie clock domain crossing** and **softcore processor reliability**. Results from previous work has resulted in the creation of a family of synchronizers to enable the crossing of clock domains in TMR systems. These synchronizers are unique in that they must correct for SEU-induced errors in the presence of asynchronous sampling uncertainty. Based on these synchronizers, we have also created a TMR asynchronous FIFO suitable for clock domain crossing as well. Additionally, our prior work identified and tested a large number (> 10) of memory mitigation strategies for use with on-chip memory structures associated with soft-core processors. These were then used in conjunction with a Picoblaze processor to demonstrate the reliability achievable. In this project we aim to extend these results in a number of ways.

In the area of softcore processors we intend to develop software-based fault mitigation techniques. These will include control flow monitoring, code redundancy, capability checks, and checkpointing. Unlike hardware-based mitigation techniques, these allow a processor to temporarily misbehave and are able to roll back the computation to a known good point after the fault has been repaired. These will be applied to an FPGA-based LEON3 softcore processor which will be adapted for this project. This will provide the ability to also evaluate combined hardware/software techniques, taking advantages of the strengths of each.

In the area of reliable data communications, we are focusing on the reliability of serial I/O-based communications on FPGAs. Modern FPGAs contain gigabit serial transceivers to enable high speed (3Gb/sec and higher) serial communications between FPGAs and also between FPGAs and other serial-connected devices. The reliability of these structures are not yet fully understood nor is the reliability of protocols and channel-bonded links based on serial transceivers. In the project we are constructing a number of serial I/O based test systems to better understand their reliability considerations. We also are developing mitigation techniques for these same systems.

## EXPERIMENTAL PLAN:

**Fault-tolerant softcore processor**: 1) Adapt the LEON3 softcore processor for use in software-based mitigation experiments, 2) Perform experiments in control flow monitoring, 3) perform experiments using code redundancy techniques, 4) perform experiments with capability checks, and 5) develop and test checkpointing mechanisms to support recovery from softcore processor failure. In steps 2) through 5) duplicated softcore processors will be employed. In steps 2) through 4) the processors will be synchronized and in step 5) they will not be synchronized.
**Reliable Serial I/O**: 1) Survey the state of the art regarding serial I/O and reliability, 2) Propose a family of reliable serial I/O systems (example: dual channel design with a single, shared mitigated protocol block), 3) Test and characterize these proposed system using simulation, hardware execution, and fault injection.

## HOW THIS PROJECT IS DIFFERENT:

Existing processors in space are slow and very expensive, since they must be radiation hardened. This project will allow softcore processors to be used in space reliably without the need for radiation hardening. Also, the reliability of serial I/O communciations is not well understood – this project will contribute to our understanding.

## POTENTIAL MEMBER COMPANY BENEFITS:

A fault-tolerant 8-bit and 32-bit softcore processor will be developed. In addition to the processor source, characterizations in terms of area, performance, power, reliability will be available. Technical reports on how to develop safe TMR designs with multiple clock domains will also be useful to members for a variety of application domains.

## EXPECTED DELIVERABLES:

1. Fault-tolerant 8-bit processor source and 32-bit processor source
2. New methodology for evaluating fault-tolerance of softcore processors
3. Reliable serial I/O based communication structure designs.
4. Technical papers and project reports

**PROJECT BUDGET:** Three memberships

**GRADUATE STUDENT PROJECT LEADERS:** Nathan Rollins and Kevin Ellsworth