CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B5b-09: Reliable Architectures for Reconfigurable Computing*

INVESTIGATOR(S) *Brent Nelson, Mike Wirthlin, Brad Hutchings*

PROJECT DESCRIPTION:

There is a growing interest in using reconfigurable devices in space-based systems. While reconfigurable systems offer great advantages, they are susceptible to single event upsets (SEUs). Thus reconfigurable systems must be made reliable in the presence of SEUs. This project investigates reliable processing in terms of **clock reliability** and **softcore processor reliability**.

The goal of the first task is to implement a **fault-tolerant sofcore processor**. Reliable softcore processors are particularly applicable to space-based applications. Currently, when processors are used in space they must be radiation hardened. Rad-hard processors are very expensive and very slow. A fault-tolerant softcore processor will be cheap, fast, and reprogrammable.

The second task is to develop safe ways for TMR to cross different **clock domains**. When TMR crosses clock domains, it suffers from the synchronization issue among its three module copies. This problem increases TMR's vulnerability to SEU's. It is necessary to create a mathematical model for the synchronization problem in order to analyze its effect. Finally, we want to propose safe ways to send control signals as well as data across different clock domains in a system with TMR.

EXPERIMENTAL PLAN:

Fault-tolerant softcore processor: 1) apply existing hardware reliability techniques (such as TMR, scrubbing, DWC, ECC) and software reliability techniques (such as control flow monitoring and checkpointing) to a softcore processor in order to improve its reliability by at least two orders of magnitude, 2) build on existing fault-tolerance evaluation methods to develop a methodology for evaluating the fault-tolerance effectiveness of reliable softcore processors. The approach that will be taken will be to start by making a small 8-bit processor (Xilinx picoBlaze) fault-tolerant, and then scale up to a larger processor.

TMR crossing clock domains: 1) build circuits with TMR and multiple clock domains, run hardware experiments to verify the mathematical model, 2) manually route the TMR circuits to determine the effects of manual routing, and further verify the correctness of the model, 3) run hardware experiments to determine whether meta-stability of flip-flops needs to be considered when solving the synchronization problem, 4) run hardware experiments to validate the proposed mitigation solutions.

HOW THIS PROJECT IS DIFFERENT:

Existing processors in space are slow and very expensive, since they must be radiation hardened. This project will allow softcore processors to be used in space reliably without the need for radiation hardening. Also, when TMR crosses multiple clock domains, synchronization issues increase its vulnerability to SEU's. This project will find appropriate solutions to solve this problem, opening up significant flexibility for designers when creating reliable FPGA-based systems.

POTENTIAL MEMBER COMPANY BENEFITS:

A fault-tolerant 8-bit and 32-bit softcore processor will be developed. In addition to the processor source, characterizations in terms of area, performance, power, reliability will be available. Technical reports on how to develop safe TMR designs with multiple clock domains will also be useful to members for a variety of application domains.

EXPECTED DELIVERABLES:

1. Fault-tolerant 8-bit processor source and 32-bit processor source
2. New methodology for evaluating fault-tolerance of softcore processors
3. Hard macro circuit designs useful for reliably crossing clock domain boundaries
4. Technical papers and project reports

PROJECT BUDGET:

Three memberships.