

CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B5a-09: Reliability Techniques for DSP/Comm Systems*

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PROJECT DESCRIPTION:

During 2008, a project was pursued within CHREC to investigate the effects of single-event upsets (SEUs) in DSP and digital communications systems on FPGAs. This project will expand on that work by developing a greater understanding of these effects and demonstrate methods to combat these radiation-induced faults. During this year the project has two emphases: **SEU-induce noise** and **detection using smart models**.

The **SEU-induced noise** task will focus on describing the effects of SEUs as noise in DSP and digital communications systems as implemented on SRAM-based FPGAs. By analyzing the types of errors produced by these effects, it should be possible to develop mitigation techniques that take advantage of the structure and algorithms utilized by these types of systems. This task will also investigate at least one possible mitigation technique: reduced-precision redundancy (RPR), evaluating its effectiveness for DSP systems and providing recommendations for its usage in these types of systems.

The **detection using smart models** task aims to research a technique to be used in place of triple modular redundancy (TMR). Using TMR, faults can automatically be masked, allowing the system to operate correctly. As is well known, TMR is costly in terms of size and power. Using simple duplication with compare (DWC), a fault can be detected but the correct circuit cannot be determined. The purpose of the smart models to be developed in this work is to choose between the outputs of a DWC circuit when they differ, by determining which copy is the non-faulty one with a high degree of accuracy. To do so these smart model will make use of various application-specific information. In this task we will research various options for smart models, demonstrate their use, and quantify the resulting circuit area and performance costs vs. savings.

EXPERIMENTAL PLAN:

SEU-Induced Noise: (1) describe the noise characteristics induced by SEUs on FPGA-based DSP and digital communications systems, (2) experiment with the noise effects of SEUs on a digital filter in a communications receiver, showing the effect on bit error rate (BER), (3) experiment with various levels of RPR and report on the effects on BER. Steps 1 and part of 2 will be completed by the June meeting. The remainder will be completed by year end.

Detection using Smart Models: (1) experiment using a simple statistical model on a simple FIR filter and characterize its performance, (2) expand this model to other basic digital communication blocks, (3) expand to other, more complex smart models (e.g. neural nets, hidden Markov models).

HOW THIS PROJECT IS DIFFERENT:

This project is a departure from standard TMR approaches, and will introduce novel techniques for mitigating the effects of SEUs in DSP and digital communications systems. The effects of SEUs in DSP systems have not previously been analyzed as noise, nor has DWC been augmented with smart models in order to reduce the cost of mitigation.

POTENTIAL MEMBER COMPANY BENEFITS:

The results of this task will provide better understanding of SEU mitigation techniques which are tailored to DSP and digital communications systems as implemented on an FPGA. By utilizing knowledge of an FPGA application, SEU protection can be realized at a lower cost than standard TMR.

EXPECTED DELIVERABLES:

1. Experimental results examining the characteristics of SEU-induced noise in FPGA DSP systems.
2. Studies of smart model options for improved fault mitigation in FPGA DSP systems.
3. Analysis of the effectiveness of the reduced-precision redundancy (RPR) in digital communications systems.
4. Demonstration of RPR and smart model-based mitigation using a fault injection simulator.
5. Project reports and technical papers.

PROJECT BUDGET:

Four memberships.