

CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B5-10: Reliability Techniques for RC Systems*

INVESTIGATOR(S) *Michael Wirthlin, Brent Nelson*

PROJECT DESCRIPTION:

During 2008 and 2009, BYU completed a project within CHREC to investigate the effects of single-event upsets (SEUs) in DSP and digital communications systems on FPGAs. These projects demonstrated that DSP and communications systems are far less sensitive to SEUs than expect. This project will expand on that work by completing a full system mitigation demonstration, testing additional higher order statistical techniques, and investigating the impact of bit-widths on reduced precision redundancy (RPR) and SEU sensitivity.

The **full system mitigation demonstration** task will test the mitigation techniques developed in previous years within a full communications receiver (demodulator plus timing recovery). This system will include feedback to test the impact of feedback on these mitigation techniques. Other signal processing architectures will be tested as time permits. A variant of this system demonstration will be prepared and uploaded to the Los Alamos National Laboratory Cibola Flight Experiment (CFE) satellite. Results from in-orbit tests will be presented.

The **higher order statistical techniques** task will investigate a new detection approach for the smart model mitigation scheme. Histogram based approaches were shown to provide reasonable results but require large memories. Higher order statistics has the potential to provide high quality error detection with less memory requirements. This task will investigate this approach with several DSP systems and compare the results with other known techniques. This task will also investigate the ability of smart models to handle the four different SEU error classifications (class1 – class4).

The final **bit-width analysis** task will develop techniques to estimate the minimum bit-width required of DSP and communication systems for use within RPR and traditional DSP systems. This task will develop a tool for analyzing the impact of bit-width on system error. This tool will be used to analyze the minimum bit-widths for RPR systems.

EXPERIMENTAL PLAN:

Full system mitigation demonstration (1) Develop a full communications receiver (demodulator with timing recovery), (2) Apply fault injection to system using the XRTC fault injection platform, (3) modify the design for use on the CFE satellite, and (4) analyze the fault injection and in orbit results. Steps 1 and part of 2 and 3 will be completed by the June meeting. The remainder will be completed by year end.

Higher order statistical techniques: (1) Experiment using a simple statistical model on a FIR filter and characterize its performance, (2) Expand model to other digital communication blocks, (3) Compare to techniques from previous year.

Bit-width Analysis: (1) Investigate the state of the art in automated bit-width analysis, (2) Implement a suite of analysis techniques in a system analysis tool, (3) Apply the tool for RPR experiments.

HOW THIS PROJECT IS DIFFERENT:

This project is a departure from standard TMR approaches, and will introduce novel techniques for mitigating the effects of SEUs in DSP and digital communications systems. The effects of SEUs in DSP systems have not previously been analyzed as noise, nor has DWC been augmented with smart models in order to reduce the cost of mitigation.

POTENTIAL MEMBER COMPANY BENEFITS:

The results of this task will provide better understanding of SEU mitigation techniques which are tailored to DSP and digital communications systems as implemented on an FPGA. The project will also provide a tool that members can use to automatically estimate system quantization error. Combined with RPR, this tool will lower the cost of SEU mitigation.

EXPECTED DELIVERABLES:

1. Experimental results of mitigation techniques for comm. receiver (fault injection and in-orbit results)
2. Studies of higher order statistics for improved fault detection in FPGA DSP systems.
3. Bit-width estimation tool for DSP and RPR systems.

PROJECT BUDGET: Two memberships.

GRADUATE STUDENT PROJECT LEADER: Brian Pratt