

CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B1-11: Rapid Implementation of High-Performance FPGA Designs*

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PROJECT DESCRIPTION:

Over the past few years the B1 project series has focused on rapid implementation techniques for FPGA systems. During 2010, project B1-10 focused on the use of precompiled hard macros to reduce FPGA synthesis and implementation time by eliminating the synthesis step entirely and reducing the complexity of place-and-route to the placement and interconnection of a small number of precompiled hardware blocks (hard macros). B1-10 demonstrated a tool called HMFlow, which reduced synthesis and implementation times by as much as 10-50x compared to the conventional Xilinx tool flow, but at the expense of a 2-4x clock rate slowdown. This project (B1-11) will investigate how the use of hard macros can preserve and encapsulate timing closure effort, making it possible for HMFlow to compile hard macro-based FPGA designs for high performance systems.

EXPERIMENTAL PLAN:

Task 1 Performance Optimized Hard Macros: In this task we will build on our B1-10 experience and develop an approach for creating placed and routed IP blocks (hard macros) specifically for high performance. This will require the extension of HMFlow's constraints when creating hard macros to enable the hard macros to be internally placed and routed to meet stringent timing constraints. We will also extend HMFlow to support System Generator subsystems to enable the creation of a wider variety of hard macros for this task.

Task 2 Assembly of Hard Macros: In this task we will develop an approach for hard macro assembly to achieve high performance timing closure. The questions to be answered in this task include: (a) Can extra pipeline registers be inserted into a design to reduce critical paths? (b) How can we reshape hard macros (move their ports) to make them run faster? (c) How do we accommodate timing variation in the FPGA fabric?

Task 3 Performance Characterization: Using the high performance hard macro cores developed in the previous tasks, we will demonstrate the clock rates that can be achieved with the new assembly techniques, which will be compared with those achieved during the B1-10 project. Experiments will be run to demonstrate the ease of use of this new technique. A set of experiments will also be created to compare and contrast the new flow with other techniques such as the Xilinx PlanAhead tool.

Task 4 Extend HMFlow: In this task we will extend the B1-10 HMFlow tool to support the newly developed hard macro generation and assembly techniques from the above tasks. It will also be extended to support Virtex-5 parts. Finally, HMFlow will be extended to enable it to accept input from a variety of different input formats via the Ogre netlist format. This will enable the use of HMFlow with tools such as LabVIEW, Ptolemy, etc.

HOW THIS PROJECT IS DIFFERENT:

Reuse for hardware is significantly behind that for software. Rather than focus on simply building core libraries, we are focusing on developing a new kind of tools framework to support extremely rapid implementation of FPGA designs based on hard macros. The resulting flow will still be compatible with the use of existing vendor tool flows for the generation of final optimized designs.

POTENTIAL MEMBER COMPANY BENEFITS:

Development of a rapid reuse tool flow for use by designers will provide greatly improved incremental design and debug capabilities compared to currently available tools.

EXPECTED DELIVERABLES:

1. A macro-based design methodology including scripts, tools, and building block libraries.
2. Demos of tools and example FPGA design implementations.
3. Project reports and technical papers.

PROJECT BUDGET: Three memberships.

GRADUATE STUDENT PROJECT LEADER: Christopher Lavin