

CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B1-10: Rapid RC Development Techniques*

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PROJECT DESCRIPTION:

During 2008 and 2009, RC module projects were pursued within CHREC, including development of (a) a library of parameterized building blocks for digital radio design, (b) extensions to the IP-XACT schema to describe the characteristics of the blocks in this reusable block library, and (c) a design entry and synthesis tool for use with the library and schema to enable rapid realization of radios. The demonstration of the value of this was done by rapidly implementing a variety of QPSK digital receivers, each possessing different area/time characteristics within a very short time frame. This project is related but focuses on drastically reducing the time required for the VHDL synthesis, map, and place and route processes (by eliminating some current steps and drastically reducing the time required for others).

This project will address this using a combination of **hard macros** as the basic design element, a **hard macro manipulation tool** and an **incremental design** tool flow. The use of hard macros for circuit building blocks will enable the VHDL synthesis and mapping steps of the tool flow to be bypassed in many instances. The proposed incremental design tool flow will require minimal portions of the tool chain to be run for many design modifications. The desired result will be that for a typical design change, a previously placed-and-routed FPGA design can be modified and a new bitstream generated within seconds, providing for a truly interactive design and debug experience, which more closely approximates the *make*-based compilation flow enjoyed by software developers than today's FPGA tool flows.

EXPERIMENTAL PLAN:

Task 1 Library Creation: we will develop an approach for developing placed/routed IP blocks (hard macros). Questions to answer include (a) how to make them suitable for rapidly stitching together into a finished design and (b) how to make them logically *and* physically parameterizable.

Task 2 Place and Route Tools: we will determine the capabilities of Xilinx tools regarding the use of placed/route hard macros, specifically how the tools handle their placement and routing. This will be done for designs containing a handful of large macros as well as for designs containing many smaller macros. Additionally we will determine the restrictions on relocating macros on the FPGA fabric.

Task 3 Tool Development: based on the results of the previous two tasks we will develop a tool flow to support hard macro based design. This will include tools for creating and manipulating hard macros and their combination into finished designs. The tool flow will contain hierarchical design features as a way of providing support for rapid incremental design and implementation.

Task 4 Radio Demonstrations: experiments targeted at the rapid implementation and debug of digital radio designs will be completed to demonstrate the capabilities of the tool flow for both initial radio design as well as for rapid design modification.

HOW THIS PROJECT IS DIFFERENT:

Reuse for hardware is significantly behind that for software. Rather than focus on simply building core libraries, we are focusing on developing a new kind of tools framework to support almost instant ECO-like design changes for debug iterations. The resulting flow will still be compatible with the use of existing timing-closure vendor tool flows.

POTENTIAL MEMBER COMPANY BENEFITS:

Development of a rapid reuse tool flow for use by designers will provide greatly improved incremental design and debug capabilities compared to currently available tools.

EXPECTED DELIVERABLES:

1. A macro-based design methodology including scripts, tools, and building block libraries.
2. Multiple digital radio designs and associated parameterized building blocks compatible with the tool flow.
3. Demos of tools and example rapid radio implementations.
4. Project reports and technical papers.

PROJECT BUDGET: Three memberships.

GRADUATE STUDENT PROJECT LEADER: Christopher Lavin