

CHREC PROJECT EXECUTIVE SUMMARY

PROJECT NAME *B1-09: Reuse Tools for RC Design*

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PROJECT DESCRIPTION:

During 2008, a project was pursued within CHREC to develop techniques to enable the reuse of libraries of building blocks for FPGA design. In this work an XML schema was developed to describe the characteristics of reusable circuit modules. This schema includes information on ports, bit widths of signals, functionality, etc. A set of tools was then developed for manipulating and parsing cell descriptions written in this schema. This project is a follow on and also focuses on design productivity. However, during this year the project has two emphases: **interface synthesis** and **rapid development of digital radios** as an application area for these techniques.

The problem being addressed in the **interface synthesis** task is this: cells developed in a particular CAD tool (VHDL for example) may not conform to the interfaces required for use in certain design environments (LabView FPGA or System Generator for example). Thus, users are required to manually "wrap" circuit modules with additional circuitry in order to use those design environments. In this task we will develop interface specifications for CAD tools and then develop automated synthesis tools which use those specifications to automatically generate wrapper circuitry.

The **radio development** task will use these reuse techniques and tools in the development of a small number of digital radios. This will allow us to test our parameterized module library and the reuse tools and techniques being developed in the project. Our final goal will be to demonstrate rapid prototyping of radio personalities by the end of the year.

EXPERIMENTAL PLAN:

Interface Synthesis: (1) develop interface specification descriptions for both LabView FPGA and System Generator, (2) develop tools able to take cells from cell library and automatically generate (synthesize) the interface circuitry required so that those cells can be used with either LabView FPGA or System Generator, (3) demonstrate these tools in the use of a variety of cells and tools without the need for the user intervention to manually create the interface circuitry required. Steps 1 and part of 2 will be completed by the June meeting. The remainder will be completed by year end.

Radio Development: (1) developing two or three one or more radio personalities taken from the set (PCM/FM, QPSK, SOQPSK) using conventional design techniques, (2) for each individual circuit module used in these radio personalities, develop a parameterized version and place into the reuse library, (3) apply the interface synthesis tools and techniques also developed in this project and demonstrate the rapid assembly of new radio personalities in an automated fashion.

HOW THIS PROJECT IS DIFFERENT:

Reuse for hardware is significantly behind that for software. Rather than focus on building core libraries, we are focusing on a framework to enable use of a variety of existing libraries with a variety of existing tools.

POTENTIAL MEMBER COMPANY BENEFITS:

Development of interface synthesis CAD tools and radio building blocks library to provide ability for rapid reuse by designers. Library and interface standards have value in promoting standard practices and tool development.

EXPECTED DELIVERABLES:

1. CAD tool interface specification descriptions for LabView FPGA and System Generator in XML format.
2. Interface synthesis tool to use and manipulate these interface specifications.
3. Multiple digital radio designs and associated parameterized building block set.
4. Demos of interface synthesis tools for rapid radio implementation.
5. Project reports and technical papers.

PROJECT BUDGET:

Three memberships.