

2008 CHREC Projects

Virginia Tech Site of CHREC

V1-08: Model-Based Engineering Framework for HPRC Applications

- *Description:* The abstraction level of Reconfigurable Computing (RC) has been stymied at the hardware design level, slowing productivity and acceptance of these devices for the wider range of applications. While devices such as FPGAs are programmable, they are treated fundamentally different than software – requiring a substantial amount of hardware design knowledge to produce. Yet, there are some advances in model-base engineering that are yielding promising results in the software community for a similar problem. This project is to explore how the use of RC patterns, separation of concerns (modeling), transformations and mappings can be used to move the abstractions to higher levels for programming RC devices in systems. Through an exploratory prototype we will examine how these concepts apply to components in a software defined radio (SDR) application. The research objective is to see where the principles hold and breakdown, and to hypothesize what promise this holds for improving RC application development productivity.
- *Goals:* (a) Explore Model-Based Engineering (MBE) in High-Performance Reconfigurable Computing; (b) Investigate methods to raise abstraction level and address relevant separation of concerns; (c) Explore methods to re-compose/generate applications via transformations and mappings
- *Challenges:* (a) Developing effective exploratory MBE prototype in a software defined radio (SDR) application; (b) Identify where MBE principles hold/breakdown; (c) Evaluate MBE for improving productivity

V2-08: Process-to-Core Mapping for Advanced Architectures

- *Description:* With a broad range of HPRC devices and capabilities coming to market, each with its respective architecture, it has become hard to determine effective process-to-core mapping(s). Tiler/OPERA and ElementCXI represent emerging architectures for HPRC with a wide range of applications, yet little is known on how to map the processes from an application to the available cores. The research objective of this project is to examine these and other emerging architectures to understand the principles to make these mappings and to experiment with ways to automate to the extent possible the elements involved. We intend to examine the implications for these in a couple of domains (i.e., SDR and Bio-informatics – mpiBLAST).
- *Goal:* (a) Investigate application hand-crafted mapping via Tiler/OPERA; (b) Define decision framework of intelligent process-to-core mapping; (c) Exercise and refine process-to-core mapping approach and decision framework.
- *Challenges:* (a) Determining key decisions in process-to-core mappings; (b) Developing canonical process-to-core mapping decision framework; (c) Developing prototype to exercise and refine the intelligent process-to-core mapping decision framework, and demonstrating it in relevant application area(s).