

## 2008 CHREC Projects

### University of Florida Site of CHREC

#### **F1-08: System-level Formulation for Algorithm/Architecture Exploration**

- *Goals:* (a) Research concepts for an RC abstraction layer featured in application formulation stage; (b) Explore methods for enhanced modeling of FPGA core designs; (c) Investigate methods to increase RC development efficiency through pattern-based design methodology
- *Challenges:* (a) Defining an abstraction layer above simulation engine to facilitate formulation and performance prediction of RC applications before design; (b) Establishing a representation and classification for design patterns

#### **F2-08: Application Performance Analysis**

- *Goal:* Productively identify and remedy performance bottlenecks in RC applications (CPUs and FPGAs) across diverse languages and systems
- *Challenges:* (a) CPU/FPGA interaction varies heavily between system and languages, making automated instrumentation and measurement difficult; (b) HLL-to-hardware mappers have an additional layer of abstraction to manage; (c) Visualizations must selectively eliminate information to highlight bottlenecks

#### **F3-08: Case Studies in Multi-FPGA Application Design**

- *Goals:* (a) Develop applications and propose design strategies for scalable architectures from case-study experience; (b) Analyze and examine available multi-FPGA platforms and tools for scalable system design
- *Challenges:* (a) Perform multilevel algorithm partitioning, analysis, and optimization for multi-FPGA systems; (b) Determine influence of application characteristics on selection of platforms, tools and languages

#### **F4-08: Reconfigurable Fault Tolerance and Partial Reconfiguration**

- *Goals:* (a) Explore mechanisms for providing dynamic or reconfigurable fault tolerance (RFT); (b) Investigate opportunities for CAD tool concepts to make partial reconfiguration (PR) design more feasible for application developers
- *Challenges:* (a) With several promising RFT mechanisms proposed in literature, practical issues and restrictions will be a main focus as this work is extended; (b) Leverage other CHREC projects that can be exploited for PR tool research

#### **F5-08: Device Characterization & Design Space Exploration**

- *Goal:* Develop fundamental research foundation to explore FPLDs, with broad investigation of emerging FPLD technologies, characterizations, application classes, and promising architecture enhancements
- *Challenges:* (a) In-depth architecture analysis on disparate suite of devices; (b) Correlation of application and device characteristics; (c) Modeling environment for future FPLD architectures