

2008 CHREC Projects

Brigham Young University Site of CHREC

B1-08: Core Library Framework for HPC/HPEC

- *Goals:* (a) Develop framework for encapsulating details of reusable circuit cores, (b) Demonstrate techniques for creating and extracting core details, (c) Demonstrate ability to use cores in multiple environments, and (d) Encourage standardization of core framework.
- *Challenges:* (a) Encapsulating core details in XML file, (b) Leveraging existing XML work such as IP-XACT, (c) Creating XML wrappers for several libraries, (d) Providing simple demonstrations of core composition and experiment with CHREC member tools.

B2-08: Heterogeneous Architectures for HPEC RC

- *Goals:* (a) Quantify performance of new building blocks (GPU, Cell, etc) for inclusion in heterogeneous RC systems, (b) Quantify interconnection tradeoffs in HPEC configurations, (c) Quantify difficulty of programming them, and (d) Investigate system support requirements for heterogeneous collections.
- *Challenges:* (a) Understanding the wide variety of alternatives available today via literature review and collection, (b) Perform device analysis and characterization followed by application analysis and characterization, (c) Develop measures of design productivity vs. performance, and (d) Propose and characterize hybrid architectures.

B3-08: High Reliability RC Design Tools and Techniques

- *Goals:* (a) Develop tools for automating insertion of SEU mitigation techniques, (b) Create community for using reliability tools, (c) Investigate and develop automated SEU estimation techniques, and (d) Develop SEU detection techniques.
- *Challenges:* (a) Move tools from BYU/LANL to open community (open source), (b) Create new software modules for SEU detection and sensitivity analysis, (c) Testing for distribution, (d) Validate via on-orbit CFE flight experiment.

B4-08: Reliable RC DSP/Comm Systems

- *Goals:* (a) Investigate application-specific techniques for DSP/communications system design, both for individual module mitigation and system-wide mitigation, (b) Investigate application-specific alternatives to TMR, (c) Validate via on-orbit CFE flight experiment, (d) Data collection via above activities.
- *Challenges:* (a) Evaluate failure modes of comm circuits on FPGA's, (b) Study and compare prior alternatives to TMR at the module and system levels, (c) Study and compare proposed auxiliary data alternative to TMR at both levels, (d) Create and test mitigated xmit and rcv modules on orbiting CFE platform.